JPEG-D

Baseline JPEG Decoder Core

The JPEG-D core is a standalone and high-performance JPEG decoder for still image and video decompression applications.

One of the fastest available JPEG decoders, the JPEG-D can decode at Full HD (1080p30) or higher rates, even in FPGA devices. Full compliance with the Baseline Sequential DCT mode of the ISO/IEC 10918-1 JPEG standard makes the JPEG-D core ideal for interoperable systems and devices. In addition to decoding standard Baseline JPEG streams, the core is also capable of decompressing the video payload of many (de facto) standard motion JPEG container formats.

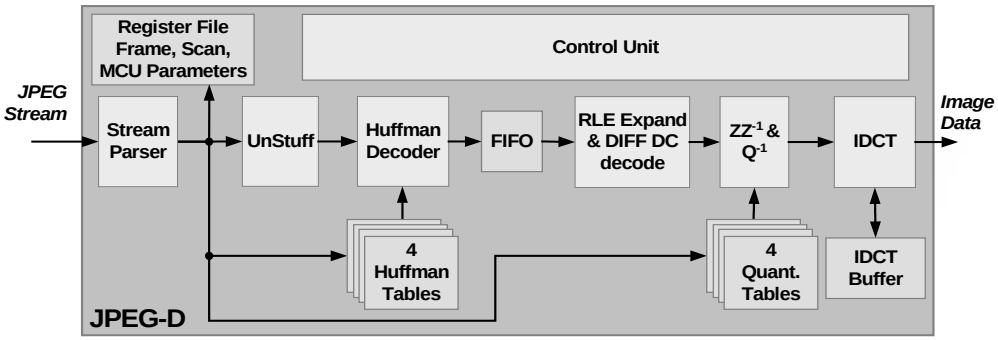
The core is designed with easy to use, fully controllable and FIFO-like, streaming input and output interfaces. Being carefully designed, rigorously verified and silicon-proven, the JPEG-D is a reliable and easy to integrate core. Its deliverables include a complete verification environment and a bit-accurate software model.

Applications

The JPEG-D core is suitable for implementing a variety of digital imaging applications, including:

- Home entertainment devices (set-top boxes, network media players etc)
- Portable multimedia devices (media players, mobile phones etc)
- Digital printing devices
- Medical imaging systems
- Video conference systems
- Surveillance systems

Block Diagram



Features

Baseline ISO / IEC 10918-1 JPEG Compliance

- Up to four Huffman Tables (two DC, two AC)
- Up to four quantization tables
- Up to four color components
- Supports all possible scan configurations and all JPEG formats for input and output data
- Supports any image size up to 64K x 64K
- Supports DNL and restart markers

Additional Processing Capabilities

- Motion JPEG payload decoding

Designed for Easy Integration

- Standalone operation
- Automatic self-programming by JPEG markers parsing
- Marker errors catching
- Broadcasting of decoded image parameters for controlling peripherals such as a block-to-raster scan converter

Designed for High Quality

- Robust verification environment includes bit-accurate software model
- ASIC and FPGA proven in multiple designs

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Functional Description

The decoding path is highly autonomous, since the JPEG-D is self-configured (with table, image format and encoding options) by parsing the incoming JPEG stream's headers. The core parses and checks all JPEG marker segments and signals in case it detects an error. Decoded image parameters are made available for controlling peripherals such as a block-to-raster converter.

Designed for continuous data flow, the JPEG-D can address the most demanding frame-based video decompression applications. Optional decoding at various resolutions from the same JPEG data-stream without the need for any extra buffering is enabled when the IDCT block is configured during synthesis to support downscaling in the frequency domain.

Support

As per the Evaluation License, support for installation and clarification of software functionality is available via email for two weeks after the core is downloaded. A commercial version with full support is also available; contact CAST Sales.

Verification

The core has been verified through extensive synthesis, place and route and simulation runs. It has also been embedded in several products, and is proven in both ASIC and FPGA technologies.

Deliverables

The core is available in ASIC (synthesizable HDL) and FPGA (netlist) forms, and includes everything required for successful implementation. The Synplicity version includes:

- HDL RTL source code.
- Sophisticated self-checking Testbench
  (Verilog versions use Verilog 2001)
- Software (C++) Bit-Accurate Model and test vector generator
- Simulation scripts, test vectors and expected results
- Synthesis sand Place and route scripts
- Comprehensive user documentation, including detailed specifications and a system integration guide

Related Megafunctions

- CMMI-JPEG Multimedia Interface – adds an AHB interface to the JPEG-D megafunction

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The JPEG-D core is sourced from
Technology Partner Alma Technologies.