



JPEG-D

Baseline JPEG Decoder Megafunction

Features

Baseline ISO/IEC 10918-1 JPEG Compliance

- Up to four Huffman Tables (two DC, two AC)
- Up to four quantization tables
- Up to four color components
- Supports all possible scan configurations and all JPEG formats for input and output data
- Supports any image size up to 64K x 64K
- Supports DNL and restart markers

Additional Processing Capabilities

- Motion JPEG payload decoding

Designed for Easy Integration

- Standalone operation
- Automatic self-programming by JPEG markers parsing
- Marker errors catching
- Broadcasting of decoded image parameters for controlling peripherals such as a block-to-raster scan converter

Designed for High Quality

- Robust verification environment includes bit-accurate software model
- ASIC and FPGA proven in multiple designs
- Easily fits most Altera device families (see implementation results table)

The JPEG-D megafunction is a standalone and high-performance JPEG decoder for still image and video decompression applications.

One of the fastest available JPEG decoders, the JPEG-D can decode at Full HD (1080p30) or higher rates, even in low-cost Cyclone-II devices. Full compliance with the Baseline Sequential DCT mode of the ISO/IEC 10918-1 JPEG standard makes the JPEG-D megafunction ideal for interoperable systems and devices. In addition to decoding standard Baseline JPEG streams, the megafunction is also capable of decompressing the video payload of many (de facto) standard motion JPEG container formats.

Evaluation designs show that the megafunction fits in a variety of Altera devices, requiring, for example, approximately 6,600 LEs for a Cyclone-III implementation. Its heavily optimized architecture enables a very high performance, reaching processing rates of up to 140 MSamples/sec in a Stratix-II device.

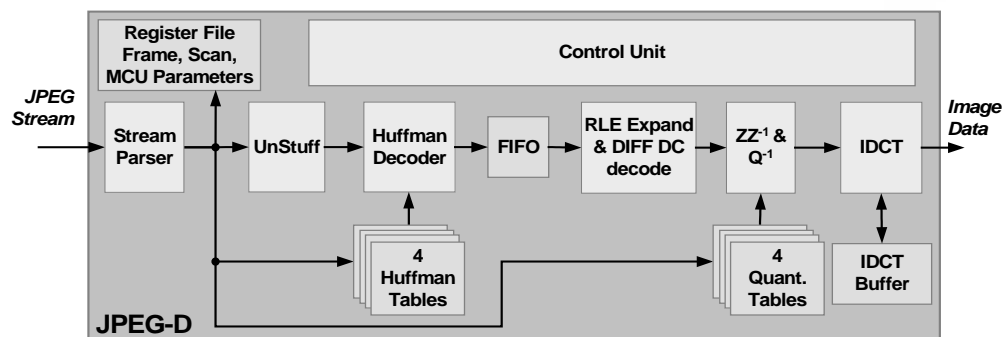
The megafunction is designed with easy to use, fully controllable and FIFO-like, streaming input and output interfaces. Being carefully designed, rigorously verified and silicon-proven, the JPEG-D is a reliable and easy to integrate megafunction. Its deliverables include a complete verification environment and a bit-accurate software model.

Applications

The JPEG-D megafunction is suitable for implementing a variety of digital imaging applications, including:

- Home entertainment devices (set-top boxes, network media players etc)
- Portable multimedia devices (media players, mobile phones etc)
- Digital printing devices
- Medical imaging systems
- Video conference systems
- Surveillance systems

Block Diagram



Functional Description

The JPEG-D is fully self-configured by parsing the marker segments that are present in the input Baseline JPEG stream. The megafunction checks also the input JPEG marker segments against errors and signals in case it detects any. The decoded image parameters are made available for controlling peripherals such as a block-to-raster scan converter.

Following the parsing of the marker segments, the JPEG-D decodes the entropy coded data segment(s) and outputs the decoded image samples in their native MCU block scan order.

Designed for continuous data flow, the JPEG-D can address the most demanding image and video decompression applications.

Implementation Results

JPEG-D reference designs have been evaluated in a variety of technologies. The following sample Altera are obtained after speed optimization during synthesis and place and route, while assuming that all megafunction I/Os are routed off-chip.

Altera Device	Logic	Fmax (MHz)	Special Features
Cyclone EP1C12-C6	8,796 LEs	85 MHz	7 M4K
Cyclone-II EP2C8-C6	6,796 LEs	112 MHz	7 M4K 19 DSP
Cyclone-III EP3C10-6	6,619 LEs	120 MHz	6 M9K 18 DSP 9-bit
Stratix EP1S10-C5	6,158 LEs	95 MHz	7 M4K / 1 M512 18 DSP
Stratix-II EP2S15-C3	6,053 ALUTs	140 MHz	7 M4K / 1 M512 18 DSP
Hardcopy-II HC210	55,220 HCELLs	192 MHz	12 M4K 36 DSP

Support

The megafunction as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Verification

The megafunction has been verified through extensive synthesis, place and route and simulation runs. It has also been embedded in several products, and is proven in both ASIC and FPGA technologies.

Deliverables

The megafunction is available in ASIC (synthesizable HDL) and FPGA (netlist) forms, and includes everything required for successful implementation. The Altera version includes:

- Post-synthesis VQM or QXP netlist
- Sophisticated self-checking Testbench (Verilog versions use Verilog 2001)
- Software (C++) Bit-Accurate Model and test vector generator
- Simulation scripts, test vectors and expected results
- Place and route scripts
- Comprehensive user documentation, including detailed specifications and a system integration guide

Related Megafunctions

- CMMI-JPEG Multimedia Interface – adds an AHB interface to the JPEG-D megafunction.