The JPEG-D-X core is a standalone and high-performance JPEG decoder that complies with both the Baseline (8-bit) and Extended Sequential (12-bit) DCT modes of the ISO/IEC 10918-1 JPEG standard.

The core’s processing throughput is sufficient for decoding multiple Full HD channels, even in FPGA devices. Full compliance with the Baseline Sequential DCT mode of the ISO/IEC 10918-1 JPEG standard makes the decoder ideal for interoperable systems and devices. In addition to decoding standard Baseline JPEG streams, the core is also capable of decompressing the video payload of many (de facto) standard motion JPEG container formats.

The core is designed with easy to use, fully controllable and FIFO-like streaming input and output interfaces. AMBA® AHB or AXI wrappers are available on request. Carefully designed, rigorously verified, and silicon-proven, the JPEG-D-X is a reliable and easy to integrate core.

Applications
The JPEG-D-X core is suitable for implementing a variety of digital imaging applications, including:
- Automotive imaging
- Medical imaging
- Machine Vision
- Surveillance

Block Diagram

Deliverables
The core is available in HDL source code or as a targeted FPGA netlist. Deliverables include everything required for successful implementation, including an extensive testbench environment, comprehensive documentation, sample scripts, and a bit-accurate software model.