

# CAST

## JPEG-C

### Baseline JPEG Codec Core

#### Features

##### JPEG Compliance

- Programmable Huffman Tables (two DC, two AC)
- Programmable quantization tables (up to four)
- Up to four color components
- Supports all possible scan configurations and all JPEG formats for input and output data
- Supports any image size up to 64K x 64K
- Supports DNL and restart markers

##### Additional Processing Capabilities

- Motion JPEG payload support
- Rate-Control (optional)

##### Designed for Easy Integration

- Standalone operation
- Simple and zero latency streaming interfaces
- Encoding Mode
  - Single clock per input sample processing rate
  - Fully programmable through standard JPEG marker segments
  - Automatic JPEG markers generation on the output
  - Automatic program-once encode-many operation
- Decoding Mode
  - Automatic self-programming by JPEG markers parsing
  - Marker errors catching
  - Broadcasting of decoded image parameters for controlling peripherals such as a block-to-raster scan converter

##### Designed for High Quality

- Robust verification environment includes bit-accurate software model
- ASIC and FPGA proven in multiple designs

The JPEG-C core is a standalone and high-performance, half-duplex, JPEG codec for still image and video compression applications.

One of the fastest available JPEG codecs, the JPEG-C can process multiple Full HD channels, even in FPGA devices. Full compliance with the Baseline Sequential DCT mode of the ISO/IEC 10918-1 JPEG standard makes the JPEG-C core ideal for interoperable systems and devices. In addition to the standard Baseline JPEG streams, the core is also capable of supporting the video payload of many (de facto) standard motion JPEG container formats. The JPEG-C can also be enhanced with an optional add-on bit-rate control block, which will benefit the bandwidth constraint applications.

Evaluation designs show that the core fits in a variety of silicon technologies, requiring, for example, approximately 95,000 gates on a 90nm process. Its heavily optimized architecture enables a very high performance, reaching processing rates beyond 300 MSamples/sec.

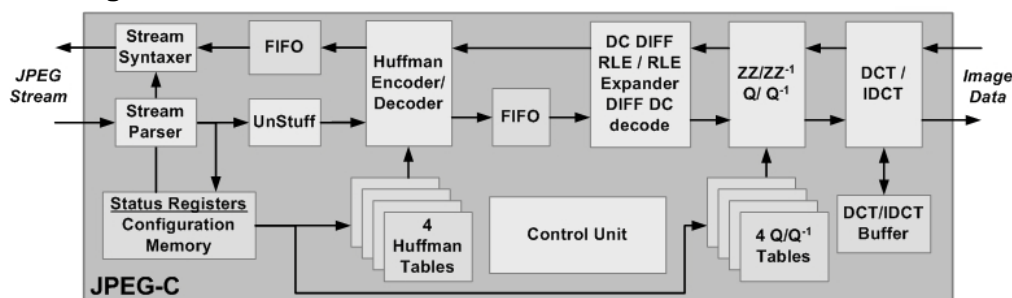
The core is designed with easy to use, fully controllable and FIFO-like, streaming input and output interfaces. Being carefully designed, rigorously verified and production-proven, the JPEG-C is a reliable and easy to integrate core. Its deliverables include a complete verification environment and a bit-accurate software model.

## Applications

The JPEG-C core is suitable for implementing a variety of digital imaging applications, including:

- Digital cameras and camcorders
- Office automation equipment (multi-function printers, scanners etc)
- Medical imaging systems
- Video conference systems
- Surveillance systems

## Block Diagram



## Functional Description

In the encoding mode the JPEG-C is configured by feeding it with JPEG headers, which contain table specification data, image format definitions and encoding options. The core's configuration can be optionally modified after the encoding of one or more frames. The image samples, in any color space, are then input to the JPEG-C in an MCU block scan order.

Consuming a single clock cycle per input image sample, the JPEG-C can address the most demanding image and video compression applications. The JPEG-C outputs a complete JPEG-compliant data stream, including JPEG headers, the size of which can be dynamically controlled when the optional rate-control block is utilized.

The decoding path is fully self-configured by parsing the marker segments that are present in the input Baseline JPEG stream. The core checks also the input JPEG marker segments against errors and signals in case it detects any. The decoded image parameters are made available for controlling peripherals such as a block-to-raster scan converter.

Following the parsing of the marker segments, the JPEG-C decodes the entropy coded data segment(s) and outputs the decoded image samples in their native MCU block scan order. Designed for continuous data flow, the JPEG-C can address the most demanding image and video decompression applications.

## Implementation Results

JPEG-C reference designs have been evaluated in a variety of technologies. The following are sample ASIC pre-layout results optimized for speed, as reported from the synthesis tool and silicon vendor design kit under typical conditions.

ASIC Technology	Logic Eq. Gates	Fmax (MHz)	Memory
UMC 0.18 $\mu$ process	104,611	220 MHz	23,360 bits
TSMC 0.09 $\mu$ process	95,348	330 MHz	23,360 bits

## Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

## Verification

The core has been verified through extensive synthesis, place and route and simulation runs. It has also been embedded in several products, and is proven in both ASIC and FPGA technologies

## Deliverables

The core is available in ASIC (synthesizable HDL) and FPGA (netlist) forms, and includes everything required for successful implementation. The ASIC version includes:

- HDL RTL source code
- Sophisticated self-checking Testbench (Verilog versions use Verilog 2001)
- Software (C++) Bit-Accurate Model and test vector generator
- Simulation scripts, test vectors and expected results
- Synthesis scripts
- Comprehensive user documentation, including detailed specifications and a system integration guide

## Related Cores

- CMMI-JPEG Multimedia Interface – adds an AHB interface to the JPEG-C core.