

Functional Description

The core is divided into five modules:

AHB Slave takes care of data transfers when accessed from the AHB bus.

AHB Master initiates data transfers on the AHB bus when directed by the DMA.

Control Register Interface implements an asynchronous clock boundary and backend register bus control.

DMA Control Registers contain a set of DMA control/status registers.

Stream-In Data FIFO buffers data processed by a multimedia core for further AHB bus transfer. It also implements an asynchronous clock boundary.

Implementation Results

CMMI reference designs have been evaluated in a variety of technologies; the results from several implementations of the core are shown below.

Configuration	Technology	Approx. Area
CMMI without DMA	TSMC 0.09 μm	12,105 gates
CMMI without DMA	TSMC 0.13 μm	13,843 gates
CMMI without DMA	TSMC 0.18 μm	14,631 gates
CMMI with 2CH DMA	TSMC 0.09 μm	16,467 gates
CMMI with 2CH DMA	TSMC 0.13 μm	18,635 gates
CMMI with 2CH DMA	TSMC 0.18 μm	19,805 gates

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Verification

The core has been verified through extensive simulation. It has also been verified in a prototyping FPGA board platform.

Deliverables

The core is available in ASIC (synthesizable) or FPGA (netlist) forms, and includes everything required for successful implementation. The ASIC version includes:

- HDL RTL source
- Sophisticated HDL Testbench including models of interfaces, and the core
- Simulation script, vectors, expected results, and comparison utility
- Synthesis script
- Comprehensive user documentation