

# CAST



## C32025TX

### Digital Signal Processor Core

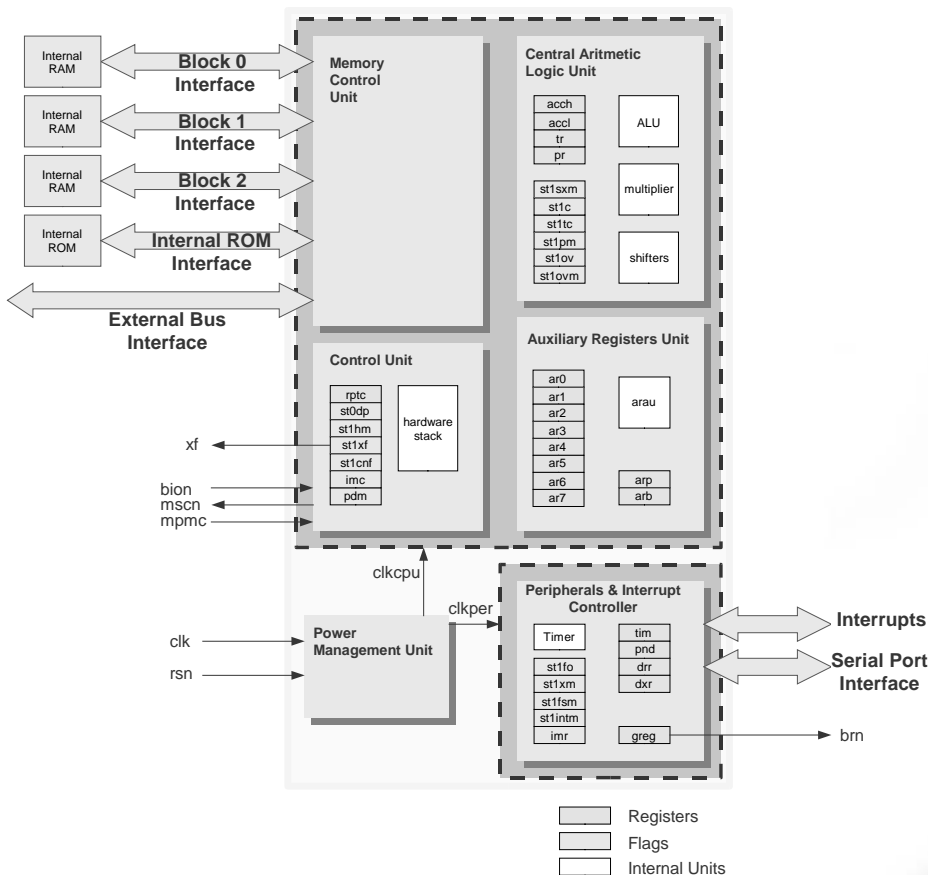
The C32025TX is a single-chip, high performance 16-bit fixed-point digital signal processor core. It implements the same instruction set as the TMS320C25 and provides the same interrupts, serial interface and timer, executing most of instructions in a single clock cycle.

The C32025TX is a microcode-free design developed for reuse in ASIC and FPGA implementations. The design is strictly synchronous with both-edge clocking, a synchronous reset, and no internal tri-states.

### Applications

- Digital sound processing (adaptive filtering, FFT, other special sound effects)
- Voice recognition
- Telecommunications (modems, codecs)
- Medical equipment (diagnostics tools)
- Computers peripherals
- Various embedded data-intensive systems

### Block Diagram



### Features

- Control Unit
  - Single-clock per machine cycle operation
  - 16-bit instruction decoding
  - Repeat instructions for efficient use of program space
  - 8-level Hardware Stack
- Central Arithmetic-Logic Unit
  - 16-bit sign-extended parallel shifter
  - 32-bit arithmetic and logical operations
  - 16 x 16 bit parallel multiplier with a 32-bit product
  - 32-bit accumulator with output shifter
  - Single-cycle Multiply-and-Accumulate instructions
- Auxiliary Registers
  - 8 x 16-bit registers for indirect addressing or data storage
  - 16-bit Auxiliary Register Arithmetic Unit including operations with reversed-carry propagation
- 16-bit reload timer
- Memory addressing modes
  - Direct – using a 9-bit Page Pointer and 7 LSBs of instruction word
  - Indirect – using Auxiliary Register File
  - Immediate – less than 16-bit via instruction word or full 16-bit long immediate following the instruction word
  - Block moves for data/program management
- Interrupt Controller
  - 6 interrupt sources plus reset and one software interrupt
- Synchronous serial port for direct codec interface
- Program Memory organization
  - 4K-words of internal ROM
  - Internal 256-word RAM block configurable either as program or data space
  - 64K-word external program space
- Data Memory organization
  - 2 Internal 256-word and one 32-word RAM blocks
  - 64K-words of external data space
  - 6 memory mapped registers

## Features (continued)

- 16 Input and 16 Output channels
- Wait states for interfacing slower off-chip devices
- Configurable synchronous/asynchronous external / internal memory support
- Power Management Unit for low-power operation
- Concurrent DMA using an extended Hold operation
- Multiprocessing support
- Global data memory interface

## Functional Description

The C32025TX core is partitioned into modules as shown in figure above and described below.

### Control Unit

Control unit consists of Program Counter (PC) and Prefetch Counter (PFC) used for program addressing and pipelining. Sequencer is responsible for data flow organization.

Repeat Counter (RPTC) is used to repeat the execution of several instructions, especially data-intensive ones.

Control Unit also contains eight-level hardware stack for PC storage during subroutine calls and interrupt service.

### Memory Control Unit

It is an interface between the processor and all on-chip or off-chip memories. There are three internal RAM blocks interfaces, internal ROM interface and external address and data buses. External wait states are possible.

### Central Arithmetic Logic Unit

Central Arithmetic-Logic Unit (CALU) consists of:

- Shifters – for sign-extended shifting
- ALU – for 32-bit arithmetic and logic operations
- Multiplier – it performs 16-bit signed or unsigned multiplication

### Auxiliary Registers Unit

Eight auxiliary registers are used for indirect data addressing or temporary data storage. Auxiliary Registers Arithmetic Unit performs operations on a current auxiliary register after each indirect data memory read/write.

### Peripherals & Interrupt Controller

There is one 16-bit continuously operating timer with programmable period. Synchronous full-duplex serial interface can be used for interfacing serial AD/DA converters and codecs.

There are three external interrupts, both edge and level triggered. Internal interrupt is generated at timer underflow or serial port after transmit/receive completion. These six interrupts are maskable using Interrupt Mask Register (IMR). There is also one non-maskable software interrupt.

### Power Management Unit

The power-down mode is invoked by executing IDLE instruction. Fetch operation is then terminated and the control unit with various other logic are suspended. Depending on the state of power down mode (PDM) status bit, only main machine clock can be disabled leaving the peripherals and interrupt controller working (PDM=1, IDLE mode), or all synchronous logic can be disabled until a hardware reset (PDM=0, STOP mode). When in power-down mode with PDM=1, any interrupt causes processor to awake.

## Performance

The architecture of C32025TX core ensures overall system speed and flexibility in processor configuration. The instruction set and control signals provide block memory transfers, communication to slower off-chip devices and multiprocessing implementations. Single-clock multiply/accumulate instructions, two large on-chip RAM blocks, eight auxiliary registers with dedicated arithmetic unit, serial interface and hardware timer make the processor appropriate for data-intensive signal processing.

The C32025TX implements Harvard-type architecture to maximize processing power by maintaining two separate program and data buses for full-speed execution. The program bus carries instructions and immediate operands while data bus interconnects various components and carries data from/to any data memory space. Both buses can carry data for single-clock multiply & accumulate operations.

Instruction flow consists of three pipeline stages, essentially invisible to a user. The pre-fetch, decode and execute stages are independent, which allows instructions to overlap. Thus, three different instructions can be active during any given cycle.

Most instructions can be used in repeat mode, when they are executed a given number of times. This feature is at most useful with block moves, multiply/accumulates, I/O transfers and table read/writes.

The table below shows the speed ratio of the C32025TX over the standard TMS320C25 chip. A speed ratio of 4 means that the C32025TX performs the same instruction four times faster than the TMS320C25.

Instruction type	Single				Repeated			
	Fastest		Average		Fastest		Average	
	clk	ratio	clk	ratio	clk	ratio	clk	ratio
Memory reference	1	4	1,9	3,1	1	4	1,1	3,9
I/O	2	2	2,1	3,7	1	4	1,7	3,6
Block transfer	4	3	4,2	3,3	1	4	1,2	4
MAC	4	3	4	4,4	1	4	1,5	4
MAC with data move	4	3	4	4,4	2	2	2	3
Other	1	4	1,6	3,9	1	4	1	4
All	1	4	1,8	3,6	1	4	1,1	3,9

## Implementation Results

The following are typical performance and utilization results using Xilinx devices. Core configured with 4096x16 ROM and 256x16 + 256x16 + 32x16 RAM.

Xilinx Device	Slices <sup>1</sup>	BRAM	DSP48	IOBs <sup>2</sup>	System Clock	ISE Version
Spartan-3E XC3S1200E-5	2347	2	-	59	45 MHz	12.1i
Spartan-6 XC6SLX150T-3	904	3	1	59	70 MHz	12.1i
Virtex-5 XC5VLX110-3	995	2	1	59	110 MHz	12.1i
Virtex-6 XC6VLX240T-3	879	4	1	59	125 MHz	12.1i

<sup>1</sup> Optimized for speed

<sup>2</sup> Assuming all I/O is routed off-chip

## Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

## Verification

The C32025TX core's functionality was verified by means of a proprietary hardware modeler. The same stimulus was applied to a hardware model that contained the original Texas Instruments TMS320C25 chip, and the results compared with the core's simulation outputs.

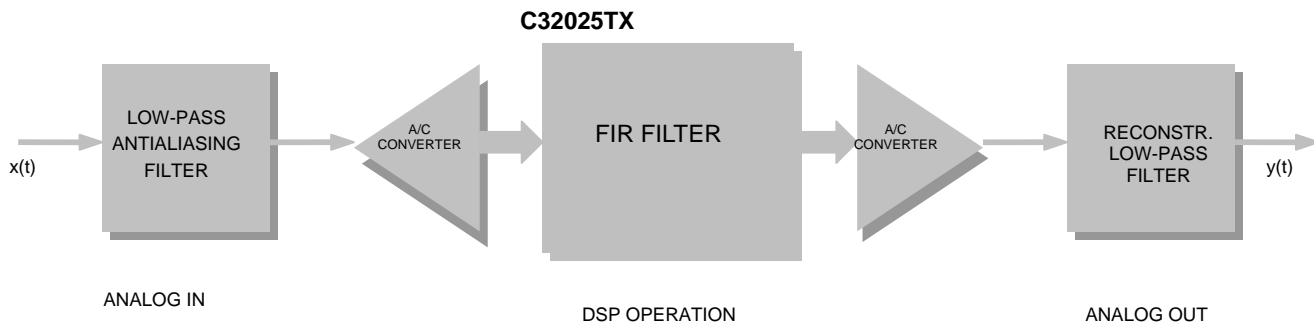
## Related Products

**C32025** – The basic version of DSP compliant with the TMS320C25 chip.

## Example Application

This application requires an analog-to-digital (A/D) converter and digital-to-analog (D/A) converter in addition to the DSP. The component count can be lower using a DSP due to the high integration available with current components in comparison to analog filter. Processing in this circuit begins by band-limiting the input with an anti-alias filter, eliminating out-of-band signals that can be aliased back into the pass band due to the sampling process. The signal is then sampled, digitized with an A/D converter, and sent to the DSP.

The filter implemented by the DSP is strictly a matter of software. The DSP can directly implement any filter that can also be implemented using analog techniques. Also, adaptive filters can be easily implemented using DSP, whereas these filters are extremely difficult to implement using analog techniques. The DSP output is processed by a D/A converter and is low-pass filtered to remove the effects of digitizing.



## Deliverables

The core includes everything required for successful implementation:

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- HDL RTL source code
- Example design showing how to connect memories and I/O buffers
- Sophisticated self-checking HDL Testbench including everything needed to test the core
- Simulation scripts, vectors, and expected results
- Synthesis script
- Comprehensive user documentation, including detailed specifications and a system integration guide