

CAST



C32025

Digital Signal Processor Core

Features

The C32025 is a 16-bit fixed-point digital signal processor core. It combines the flexibility of a high-speed controller with the numerical capability of an array processor. The C32025 has the same instruction set as the TMS320C25 and also provides the same interrupts, serial interface and timer.

The architecture of the C32025 ensures overall system speed and flexibility in processor configuration. The instruction set and control signals provide block memory transfers, communication to slower off-chip devices and multiprocessing implementations. Single-cycle multiply/accumulate instructions, two large on-chip RAM blocks, eight auxiliary registers with a dedicated arithmetic unit, serial interface and a hardware timer make the processor appropriate for data-intensive signal processing.

The C32025 implements Harvard-type architecture to maximize processing power by maintaining two separate program and data buses for full-speed execution. The program bus carries the instructions and immediate operands while the data bus interconnects various components and carries data from/to any data memory space. Both buses can carry data for multiply/accumulate single-cycle operations.

Instruction flow consists of three pipeline stages, essentially invisible to the user. The pre-fetch, decode and execute operations are independent, that allows instruction executions to overlap. Thus, three different instructions can be active during any given cycle.

Most instructions can be used in repeat mode, when executed a given number of times. This feature is most useful with block moves, multiply/accumulates, I/O transfers and table read/writes.

Developed for easy reuse with ASICs or FPGAs, the core requires under 18000 ASIC gates.

Applications

The C32025 can be utilized for a variety of digital signal processing applications including:

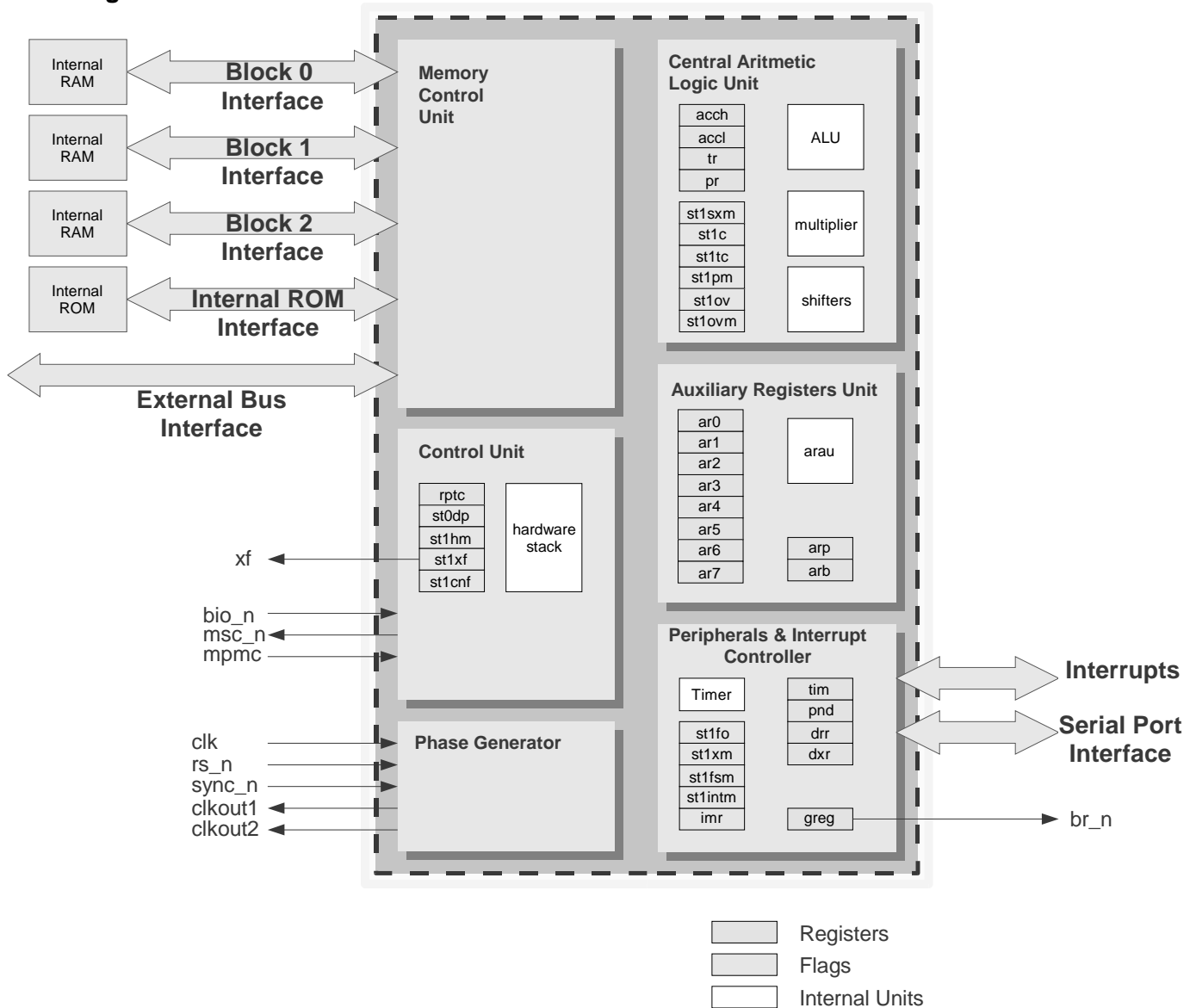
- Digital sound processing (adaptive filtering, FFT, other special sound effects)
- Voice recognition
- Telecommunications (modems, codecs)
- Medical equipment (diagnostics tools)
- Computers peripherals
- Various embedded data-intensive systems

- Control Unit
 - 16-bit instruction decoding
 - Repeat instructions for efficient use of program space and enhanced execution
- Central Arithmetic-Logic Unit
 - 16-bit parallel shifter; 32-bit arithmetic and logical operations
 - 16 x 16 bit parallel multiplier with a 32-bit product
 - 32-bit accumulator with output shifter
 - Single-cycle Multiply-and-Accumulate instructions
- Auxiliary Registers
 - 8 16-bit registers for indirect addressing or temporary data storage
 - 16-bit Auxiliary Register Arithmetic Unit including operations with reversed-carry propagation
- Memory addressing modes
 - Direct - using a 9-bit Page Pointer and instruction word's lowest 7-bits
 - Indirect - using the Auxiliary Register File
 - Immediate - less than 16-bit via instruction word or full 16-bit long immediate following the instruction word
 - Block moves for data/program management
- 8-level Hardware Stack
- Interrupt Controller: 6 interrupt sources, excluding reset and a software interrupt
- Synchronous serial port for direct codec interface
- 16-bit reload timer
- Program Memory organization
 - 4K-words of internal ROM
 - Internal 256-word RAM block configurable either as program or data space
 - 64K-word external program space
- Data Memory organization
 - 2 Internal 256-word and one 32-word RAM blocks
 - 64K-words of external data space
 - 6 memory mapped registers

Features continued

- 16 Input and 16 Output channels
- Wait states for interfacing slower off-chip devices
- Multiprocessing support
 - Global data memory interface
 - Synchronization input for synchronous multiprocessor configurations
- Concurrent DMA using an extended Hold operation
- Design is strictly synchronous with positive-edge clocking and synchronous reset, no internal tri-states.

Block Diagram



Functional Description

Control unit consists of Program Counter (PC) and Prefetch Counter (PFC) used for program addressing and pipelining. Sequencer is responsible for data flow organization. Repeat Counter (RPTC) is used to repeat the execution of several instructions, especially data-intensive ones.

Memory Control Unit

It is an interface between the processor and all on-chip or off-chip memories. There are three internal RAM blocks interfaces, internal ROM interface and external address and data buses. External wait states are possible.

Central Arithmetic Logic Unit

Central Arithmetic-Logic Unit. (CALU) consists of:

- Shifters – for sign-extended shifting
- ALU – for 32-bit arithmetic and logic operations
- Multiplier – it performs 16-bit signed or unsigned multiplication

Auxiliary Registers Unit

Eight auxiliary registers are used for indirect data addressing or temporary data storage. Auxiliary Registers Arithmetic Unit performs operations on current auxiliary register after each indirect data memory read/write.

Peripherals & Interrupt Controller

There is one 16-bit continuously operating timer with programmable period. Synchronous full-duplex serial interface can be used for interfacing serial AD/DA converters and codecs.

There are three external interrupts, both edge and level triggered. Internal interrupt is generated at timer underflow or serial port after transmit/receive completion. These six interrupts are maskable using Interrupt Mask Register (IMR). There is also one non-maskable software interrupt.

Phase Generator

Internal clock cycle divider. Machine cycle consists of four main clock cycles.

Reset input is sampled once a machine cycle and distributed all over the core.

Implementation Results

C32025 reference designs have been evaluated in a variety of technologies. The following are sample Xilinx results optimized for speed. If all I/Os are routed off chip additional IOBs are required.

Supported Family	Slices	GCLK	IOBs	Fmax (MHz)
Spartan-3E 3S1600E-5	2949	1	60	70
Virtex-4 4VLX25-12	2828	1	60	102
Virtex-5 5VLX30-3	1114	1	60	195

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Verification

The C32025 core's functionality was verified by means of a proprietary hardware modeler. The same stimulus was applied to a hardware model that contained the original Texas Instruments TMS320C25 chip, and the results compared with the core's simulation outputs.

Performance

The architecture of C32025 core ensures overall system speed and flexibility in processor configuration. The instruction set and control signals provide block memory transfers, communication to slower off-chip devices and multiprocessing implementations. Single-cycle multiply/accumulate instructions, two large on-chip RAM blocks, eight auxiliary registers with a dedicated arithmetic unit, serial interface and a hardware timer make the processor appropriate for data-intensive signal processing.

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The C32025 core is a technology independent design that can be implemented in a various processes.

Configurability

The product is delivered in the standard configuration but it may be developed according to the user's application.

Verification Methods

The C32025 core's functionality was verified by means of a proprietary hardware modeler. The same stimulus was applied to a hardware model that contained the original Texas Instruments TMS320C25 chip, and the results compared with the core's simulation outputs.

Deliverables

The core is available in ASIC (synthesizable HDL) and FPGA (netlist) forms, and includes everything required for successful implementation. The Xilinx version includes:

- Post-synthesis EDIF netlist
- Example CHIP_C32025 – TMS320C25 compatible design. This design uses the C32025 and illustrates how to build and connect memories and tri-state buffers
- Sophisticated HDL Testbench including vectors that instantiates:
 - Example design CHIP_C32025
 - External RAM
 - External ROM
 - External I/O
 - Clock generator
 - Process that compares your simulation results with the expected results

- A collection of test assembler programs which are executed directly by the Test Bench
- Simulation script, vectors, expected results, and comparison utility
- Place and route script
- Comprehensive user documentation, including architectural overview, hardware description, user guide, design support including consultation

Related Products

C32025TX – The improved and faster version of C32025. The machine cycle has been reduced from four to one clock. The same instruction set as C32025.

Example Application

This application requires an analog-to-digital (A/D) converter and digital-to-analog (D/A) converter in addition to the DSP. The component count can be lower using a DSP due to the high integration available with current components in comparison to analog filter. Processing in this circuit begins by band-limiting the input with an anti-alias filter, eliminating out-of-band signals that can be aliased back into the pass band due to the sampling process. The signal is then sampled, digitized with an A/D converter, and sent to the DSP.

The filter implemented by the DSP is strictly a matter of software. The DSP can directly implement any filter that can also be implemented using analog techniques. Also, adaptive filters can be easily implemented using DSP, whereas these filters are extremely difficult to implement using analog techniques. The DSP output is processed by a D/A converter and is low-pass filtered to remove the effects of digitizing.

