This DMA IP core implements a configurable, single-channel, direct memory access controller for the 32-bit wide AHB bus. It conforms to the Advanced Microcontroller Bus Architecture 2.0 (AMBA) specification.

The DMA32 controller contains useful features such as incrementing and non-incrementing addressing, linked list operation, and interrupt control to alert the processor to the DMA's status.

Non-incrementing addressing is useful for transferring data to and from peripherals with FIFOs or a single data port. Incrementing addressing is useful for transferring data to and from memories or peripherals containing memory. Linked list support is useful for non-contiguous memory transfer operations.

The DMA32 controller acts as a bus master device that controls data block transfers from a source memory or peripheral to a destination memory or peripheral. The controller can implement multiple DMA channels simply by instantiating more than one controller on the AMBA AHB bus. Arbitration is handled by the AHB system bus.

Applications

The DMA32 controller is suitable for a variety of applications requiring data transfers without the use of a processor such as:
- Microprocessor subsystems (specifically AMBA 2.0 AHB systems)
- Display systems
- USB, Ethernet, and Serial Communications
- Encryption/Decryption systems
- Data processing

Block Diagram
Implementation Results

DMA32 reference designs have been evaluated in a variety of technologies. The following are sample Xilinx results.

<table>
<thead>
<tr>
<th>Device</th>
<th>Slices</th>
<th>BRAM</th>
<th>IOB</th>
<th>Fmax</th>
<th>ISE Version</th>
</tr>
</thead>
<tbody>
<tr>
<td>Spartan-3 3S1500-5</td>
<td>1627</td>
<td>-</td>
<td>198</td>
<td>47 MHz</td>
<td>12.2i</td>
</tr>
<tr>
<td>Spartan-6 6SLX100-3</td>
<td>903</td>
<td>-</td>
<td>198</td>
<td>91 MHz</td>
<td>12.2i</td>
</tr>
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<td>Virtex-5 5VLX85-3</td>
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<td>-</td>
<td>198</td>
<td>143 MHz</td>
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<td>Virtex-6 6VLX7ST-3</td>
<td>737</td>
<td>-</td>
<td>198</td>
<td>193 MHz</td>
<td>12.2i</td>
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</table>

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available; contact CAST Sales.

Verification

The core has been verified through extensive simulation and system level prototyping using ARM based systems. It has also been successfully embedded in several products.

Deliverables

The core is available in ASIC (synthesizable Verilog) or FPGA (netlist) forms, and includes everything required for successful implementation. The Xilinx version includes:

- Post-synthesis EDIF netlist
- AMBA Bus Functional Model (Verilog)
- Sophisticated self-checking Testbench (Verilog)
- Simulation script, vectors, expected results, and comparison utility;
- Place and route script
- Comprehensive user documentation, including detailed specifications, software guide, and a system integration guide

Related Platforms and Cores

Platforms
- PiP-AMBA Platform

Cores
- AHB Channel
- APB Channel
- AMBA AHB to APB bridge
- AHB Arbiter
- AHB External Bus Interface
- AHB Internal Synchronous SRAM Controller
- AHB Interrupt Controller
- AHB TFT LCD Controller
- AHB STN LCD Controller
- APB General Purpose IO
- APB Parallel-Printer Port
- APB Pulse Width Modulator
- APB Real Time Clock
- APB Counter-Timer
- APB 16450/16550 Compatible UART
- APB Watchdog Timer