ZipAccel-D

GUNZIP / ZLIB / Inflate Data Decompression Core

ZipAccel-D is a custom hardware implementation of a lossless data decompression engine that complies with the Inflate/Deflate, GZIP/GUNZIP, and ZLIB compression standards.

The core features fast processing, with low latency and high throughput. On average the core outputs three bytes of decompressed data per clock cycle, providing over 3Gbps in most Altera devices. Designers can scale the throughput further by instantiating the core multiple times to achieve throughput rates exceeding 100Gbps. The latency is in the order of few tens of clock cycles for blocks coded with static Huffman tables, and typically less than 2,000 cycles for block encoded with dynamic Huffman tables.

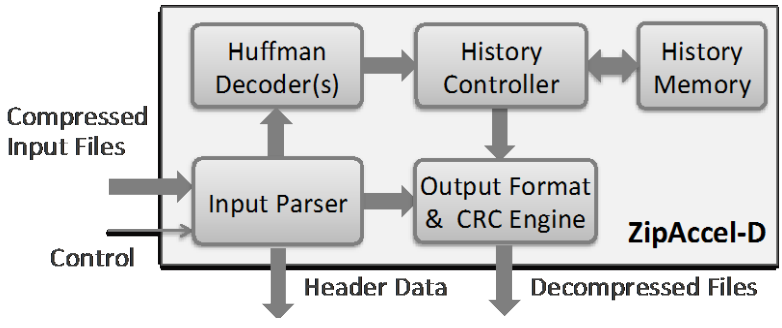
The decompression core has been designed for ease of use and integration. It operates on a standalone basis, off-loading the host CPU from the demanding task of data decompression. The core receives compressed input files and outputs decompressed files. No preprocessing of the compressed files is required, as the core parses the file headers, checks the input files for errors, and outputs the decompressed data payload. Featuring extensive error tracking and reporting errors, the core enables smooth system operation and error recovery, even in the presence of errors in the compressed input files. Furthermore, internal memories can optionally support Error Correction Codes (ECC) to simplify achievement of Enterprise Class reliability requirements.

The ZipAccel-D core is a microcode-free design developed for reuse in ASIC and FPGA implementations. Streaming data, optionally bridged to AMBA AXI4-stream, interfaces ease SoC integration. Technology mapping is straightforward, as the design is scan-ready, microcode-free, and uses easily replaceable, generic memory models. The core has been rigorously verified and production proven in a number of commercially available products.

Applications

The ZipAccel-D core is ideal for increasing the bandwidth of optical, wired or wireless data communication links, and for increasing the capacity of data storage in a wide range of devices such as networking interface/routing/storage equipment, data servers, or SSD drives. The core can also help reduce the power consumption and bandwidth of centralized memories (e.g. DDR) or interfaces (e.g. Ethernet, Wi-Fi) in a wide range of SoC designs.

Block Diagram



Features

Compression Standards

- ZLIB (RFC-1950)
- Inflate/Deflate (RFC-1951)
- GZIP/GUNZIP (RFC-1952)

Inflate/Deflate Features

- Up to 32KB history widow size
- All deflate block types
  - Static and Dynamic Huffman-Coded blocks
  - Stored Deflate Blocks

High Performance & Low Latency

- Three bytes per clock average processing rate, for throughputs exceeding 3Gbps in most Altera FPGAs with a single core, and scalable to more than 100Gbps with multiple coe instances
- Latency from a 20 clock cycles for Static Huffman blocks, and typically less than 2000 cycles for Dynamic Huffman Blocks

Easy to Use and Integrate

- Processor-free, standalone operation
- Extensive Error Catching & Reporting for Smooth Operation and Recovery in the presence of Errors
  - Header Syntax Errors
  - CRC/Adler 32 Errors
  - File Size Errors
  - Coding errors
  - Huffman Tables Errors
  - Non-correctable ECC memory errors
- Optional ECC memories, necessary for Enterprise-Class RASM
- Streaming-capable, optionally bridged to AMBA AXI4-Stream interfaces

Configuration Options

- Synthesis time configuration options allow fine tuning the core's size and performance:
  - Input and output bus width
  - FIFO sizes
  - Maximum History Window
  - Static-Only or Dynamic and Static Huffman Tables support
- Two or three decompressed bytes per cycle throughput

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Performance and Area

ZipAccel-D silicon resources requirements and throughput depends on its configuration. Also ZipAccel-D performance can scale by instantiating more Huffman decoders and by using multiple core instances.

The following are sample implementation results for different configurations of the core on an Arria10 device, and do not represent the smallest possible area requirements nor the highest possible clock frequency.

Family / Device	Huffman Tables	History Window	Freq. (MHz)	ALMs	Memory Bits	Gbps
Arria10 GX-1150	Dynamic	512	135	7,348	154,178	3.24
	Dynamic	1,024	135	7,470	158,786	3.24
	Dynamic	2,048	135	7,334	171,074	3.24
	Dynamic	4,096	135	7,329	187,714	3.24
	Dynamic	8,192	135	7,378	220,738	3.24
	Dynamic	16,384	135	7,360	286,530	3.24
	Dynamic	32,768	130	7,385	417,858	3.12
	Static	512	160	4,914	25,680	3.84
	Static	1,024	160	5,012	30,288	3.84
	Static	2,048	135	4,824	42,576	3.24
	Static	4,096	160	4,862	59,216	3.84
	Static	8,192	125	4,882	92,240	3.00
	Static	16,384	140	4,917	158,032	3.36
	Static	32,768	155	4,957	289,350	3,72

Contact CAST Sales for help defining likely configuration options and estimating implementation results for your specific system.

Verification

The core has been verified through extensive synthesis, place and route, and simulation runs. It has also been embedded in several commercially-shipping products, and is proven in both ASIC and FPGA technologies.

The core has been verified for interoperability with a number of software applications that use GZIP, ZLIB, or deflates compression.

Deliverables

The core is available in ASIC (synthesizable HDL) and FPGA (netlist) forms, and includes everything required for successful implementation. The ASIC version includes:

- HDL (Verilog) RTL source code
- Sophisticated Test Environment
- Simulation scripts, test vectors and expected results
- Synthesis script
- Comprehensive user documentation

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Related Cores

- ZipAccel-C: GZIP/ZLIB/Deflate Data Compression Core

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Sandgate Technologies

The core is sourced from Technology Partner Sandgate Technologies.