GZIP-RD-XIL

GZIP & GUNZIP Accelerator Reference Design for Xilinx

The GZIP-RD-XIL is a reference design for a PCIe data compression and decompression acceleration card using the ZipAccel-C and ZipAccel-D GZIP/ZLIB/Deflate Compression and Decompression IP Cores.

The accelerator is highly efficient and can compress data at rates exceeding 90 Gbps, making it suitable for servers or databases where it optimizes storage requirements or network bandwidth.

The reference design uses Xilinx® DMA for PCIe subsystem (XDMA) and can be mapped on Xilinx Alveo Data Center Accelerator Cards and other PCIe boards hosting 7-series, UltraScale™ or UltraScale+™ devices. The following table summarizes available off-the-shelf configurations for Xilinx FPGA boards:

Board	Function	History Window	Huffman Tables	# Cores	C/R	Gbps	FPGA Resources			
							LUT	BRAM	URAM	DSP
KCU105	Compress	32k	Dynamic	1	3.74	1.0	87k	278	0	1
KCU105	Compress	16K	Dynamic	2	3.38	11.8	211k	562	0	2
VCU1525	Compress	32k	Dynamic	4	3.64	31.2	706k	1918	144	4
VCU1525	Compress	8K	Dynamic	4	3.38	76.1	869k	1156	216	8
ALVEO-U200	Compress	32k	Dynamic	4	3.49	42.8	757k	1694	224	8
ALVEO-U200	Compress	512	Dynamic	4	3.18	92.2	607k	1336	192	16
ALVEO-U200	Compress	1024	Static	4	2.35	94.0	634K	854	192	0
ALVEO-U200	Decompress	32k	Dynamic	4	N/A	27.0	130k	188	0	0
ALVEO-U200	Decompress	32k	Dynamic	8 (*)	N/A	42.0	193k	450	0	0

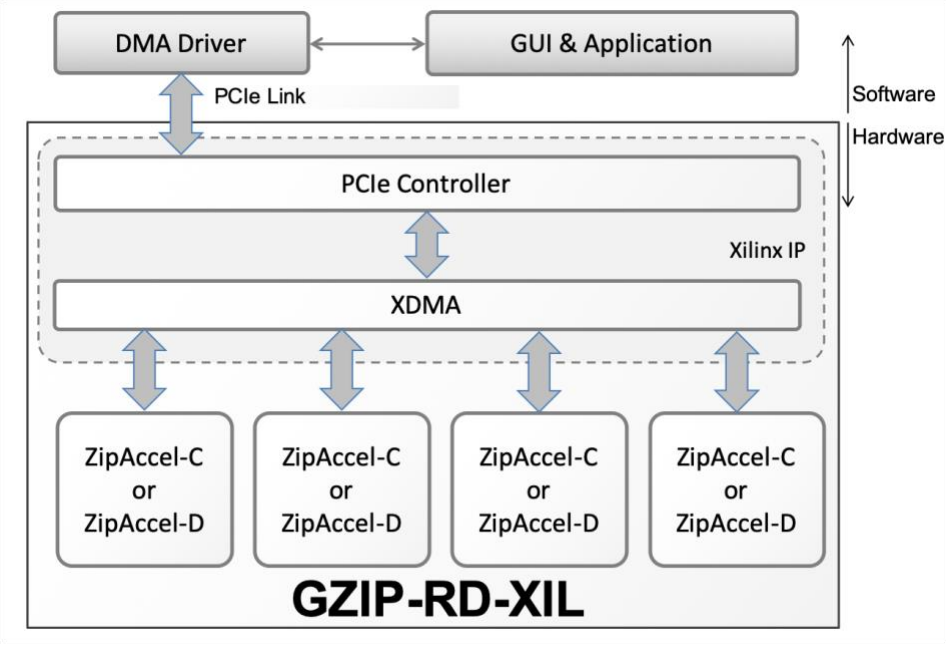
1. Table does not include all core's configuration parameters. The list of configurations is not exhaustive.
2. Compression ratio and throughput for Canterbury corpus.
(*) Decompression engine limited to operate on 64K files, and 2 cores per channel

The accelerator's compression engines, the ZipAccel-C and ZipAccel-D IP cores, are highly configurable and can be tuned to meet different application requirements with respect to silicon resources utilization, compression efficiency, and throughput. CAST will work with you to define the cores' configuration that meets your application requirements.

The reference design is delivered with a sample GUI-driven application, which designers can use to evaluate the performance of the ZipAccel-C and ZipAccel-D cores or as a basis to develop their own application.

Deliverables include the firmware (FPGA programming file), software (drivers & sample application), and comprehensive documentation, but please note that the FPGA board has to be purchased separately.

For more information please contact CAST sales.



FEATURES

Reference design of a GZIP & GUNZIP acceleration card for Xilinx FPGAs

Throughput

- Scalable and only limited by silicon resources and/or PCIe throughput
- Over 90 Gbps uncompressed data rate on Alveo and VCU15125

Compression Efficiency

- Configurable and up to software gzip level - 6

FPGA Boards

- Xilinx Alveo™ boards
- Xilinx Kintex UltraScale FPGA KCU105 Evaluation Kit
- Xilinx Virtex UltraScale+ FPGA VCU1525 Acceleration Development Kit
- Alpha Data ADM-PCIE-KU3 HPC Board
- Design portable to other boards and FPGA families

Software

- Drivers for Linux Fedora-26 (portable to other Operating Systems on request)
- Sample Application

Third-Party IP Cores

- Xilinx IP
  - PCIe End Point controller
  - DMA for PCIe subsystem

www.cast-inc.com • info@cast-inc.com • tel +1 201.391.8300

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