GZIP-RD-INT

GZIP & GUNZIP Accelerator Reference Design for Intel FPGAs

The GZIP-RD-INT is a reference design of an accelerator for GZIP data compression and decompression. The reference design is available for PCIe cards hosting Intel® Arria® 10 or Statix® 10 FPGAs.

It uses CAST's ZipAccel-C and ZipAccel-D GZIP/ZLIB/Deflate Compression and Decompression IP Cores and Intel's PCI Express and DMA IP cores, and it Is provided with software drivers and a sample Linux application. Developers can use the sample application to evaluate the performance of the IP cores or as a basis to build their own FPGA-accelerated application.

The ZipAccel-C and Zipaccel-D IP cores are highly configurable and can be tuned to meet different application requirements with respect to compression efficiency, latency and throughput. Versions for Intel Arria® 10 and Startix® 10 FPGAs, using different configurations of the ZipAccel IP cores are readily available, and CAST will work with you to define the configuration that meets your application requirements.

GZIP-RD-INT for Arria 10 FPGAs

Several reference design configurations for the Intel® Programmable Acceleration Card (PAC) with Intel Arria 10 GX FPGA are available off the shelf. A subset of these configurations is provided below:

AFU Function	History Window	Huffman Tables	# Search / # Huffman	C/R[1]	Gbps[1]	Arria 10 GX 1150 Resources	
						ALMs	Mem. Bits
Compression	32KB	Dynamic & Static	1/1	3.76	1.28	20%	17%
Compression	32KB		10/2	3.49	12	40%	49%
Compression	4KB		16/4	3.32	17.9	50%	38%
Compression	1KB		20/10	3.22	41	71%	56%
Compression	512B	Static	18/6	2.26	43.5	40%	34%
Decompression	32KB	Dynamic & Static	N/A	N/A	4.4	14%	3%

1: Compression Ratio and Throughput for the Canterbury Corpus

The Arria 10 reference design is based on Intel Streaming DMA AFU reference design and uses the related Intel DCP drivers. Developers can therefore benefit from the integration with Intel Acceleration Stack for Intel Xeon CPU with FPGAs, which greatly simplifies the use of FPGA acceleration in Xeon-based systems.

GZIP-RD-INT for Stratix 10 FPGAs

The GZIP-RD-INT is also available as an accelerator function for the Stratix 10 GX FPGA Development Kit, where it can compress or decompress data at rates exceeding 80 Gbps. This Stratix-10 reference design is delivered with the same software application as for Arria 10, which in this case does not use the DCP drivers, but rather the drivers for the Intel's Multi-Channel DMA for PCI Express IP core. The Stratix 10 reference design can be ported to other boards hosting Intel Stratix 10 FPGAs.

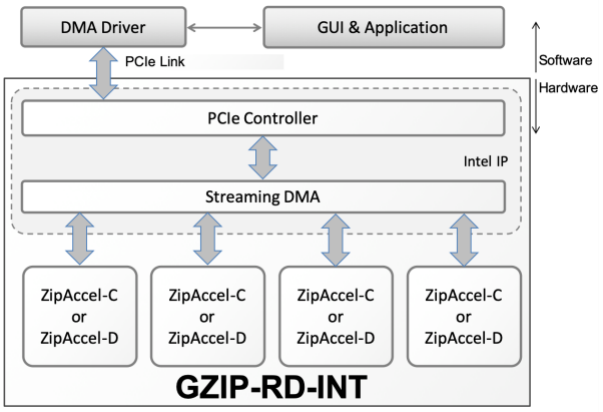
Deliverables

Deliverables include the firmware (FPGA programming file), software (drivers), and comprehensive documentation, but please note that the FPGA boards d licenses for the Intel IP cores and Intel software have to be acquired separately.

Support

The reference design as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

For more information please contact CAST sales.



FEATURES

PCIe board data compression reference design for evaluating or developing with ZipAccel Compression or Decompression Cores

GZIP Acceleration

- Over 40 Gbps uncompressed data rate on Intel PAC with Intel Arria 10 GX FPGA
- Over 80 Gbps on Stratix 10 GX Development Kit
- High compression efficiency (comparable to software gzip-6)
- Fully Compliant to the GZIP standard (RFC-1952)

Supported Hardware

- Intel Programmable Acceleration Card (Intel PAC) with Intel Arria 10 GX FPGA
- Stratix 10 GX FPGA Development Kit
- Design portable to other Arria 10 or Stratix 10 boards on request

Software

- Sample GUI-Driver or command-line Linux application
- Intel® Acceleration Stack for Intel Xeon® CPU (from Intel)
- MCDMA Drivers for Stratix 10 (from Intel)

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