HSDLC
HDLC & SDLC Protocol
Controller Core

The HSDLC IP core implements a controller for the High-Level Data Link Control (HDLC) and the Synchronous Data Link Control (SDLC) protocols. It is based on the Intel 8XC152 Global Serial Channel (GSC) working in SDLC mode, and adds features to support HDLC or proprietary frame transmission under host processor control.

The core operates as a peripheral to a host processor, and is easy to integrate with both modern and legacy processors. Control and status registers are accessible via an APB or a generic 80c51-like bus interface, and a comprehensive set of interrupt signals facilitates interrupt-based operation.

The controller’s great flexibility enables a variety of serial link setups. It provides two independent interfaces, one for transmitting and one for receiving data. Both interfaces provide control signals for the link drivers to support both full- and half-duplex operation. The controller can be programmed to use hardware flow control signals (RTS/CTS) and it can also detect collisions. The baud-rate is programmable and limited only by the link drivers and the core’s clock frequency. The core derives the receive clock from the received serial data, or uses an externally provided receive clock.

The HSDLC controller core is designed for reuse and is rigorously verified and scan-ready. Although designed to manage serial links, the core contains no latches or tri-states, and is fully synchronous with a single clock domain. The core is available in Verilog RTL or as a targeted FPGA netlist. Deliverables provide everything required for a successful implementation, including sample scripts, an extensive testbench, and comprehensive documentation.

Applications
The HSDLC controller core be used in telecommunication equipment supporting HDLC-based protocols such as X.25 or ISDN-D. It can also be used to implement serial interfaces between processors and peripherals.

Block Diagram
Support
The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Implementation Results
HSDLC core reference designs have been evaluated in a variety of technologies. The following are sample results, for the core configured with Tx and Rx FIFOs. FIFOs are 3 bytes each and implemented with flip-flops.

<table>
<thead>
<tr>
<th>Technology</th>
<th>Area (eq. NAND2 gates)</th>
<th>Max. Freq. (MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TSMC 65nm LP</td>
<td>7,575</td>
<td>400</td>
</tr>
<tr>
<td>TSMC 40nm G</td>
<td>5,594</td>
<td>1,200</td>
</tr>
<tr>
<td>TSMC 28nm HPM</td>
<td>4,588</td>
<td>1,800</td>
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Verification
The HSDLC core has been verified through extensive simulation and rigorous code coverage measurements.

Deliverables
The core includes everything required for successful implementation:
- Verilog RTL source code
- Post-synthesis EDIF (netlist licenses)
- Testbenches
- Simulation scripts
- Synthesis scripts
- Documentation