HSDLC

HDLC & SDLC Protocol Controller Core

The HSDLC IP core implements a controller for the High-Level Data Link Control (HDLC) and the Synchronous Data Link Control (SDLC) protocols. It is based on the Intel 8XC152 Global Serial Channel (GSC) working in SDLC mode, and adds features to support HDLC or proprietary frame transmission under host processor control.

The core operates as a peripheral to a host processor, and is easy to integrate with both modern and legacy processors. Control and status registers are accessible via an APB or a generic 80c51-like bus interface, and a comprehensive set of interrupt signals facilitates interrupt-based operation.

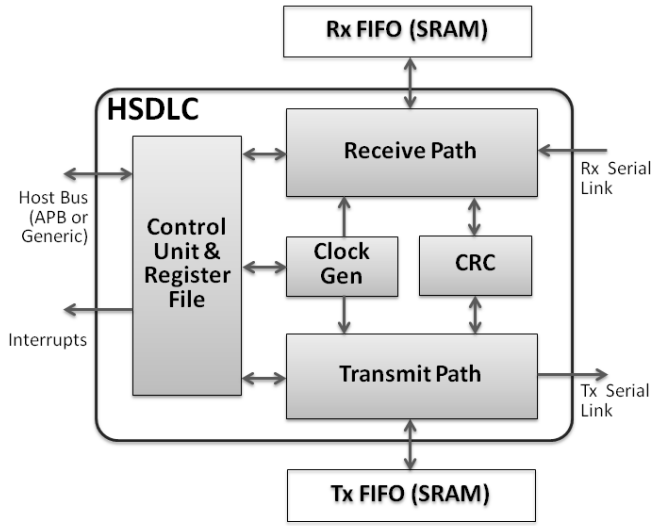
The controller's great flexibility enables a variety of serial link setups. It provides two independent interfaces, one for transmitting and one for receiving data. Both interfaces provide control signals for the link drivers to support both full- and half-duplex operation. The controller can be programmed to use hardware flow control signals (RTS/CTS) and it can also detect collisions. The baud-rate is programmable and limited only by the link drivers and the core's clock frequency. The core derives the receive clock from the received serial data, or uses an externally provided receive clock.

The HSDLC controller core is designed for reuse and is rigorously verified and scan-ready. Although designed to manage serial links, the core contains no latches or tri-states, and is fully synchronous with a single clock domain. The core is available in Verilog RTL or as a targeted FPGA netlist. Deliverables provide everything required for a successful implementation, including sample scripts, an extensive testbench, and comprehensive documentation.

Applications

The HSDLC controller core be used in telecommunication equipment supporting HDLC-based protocols such as X.25 or ISDN-D. It can also be used to implement serial interfaces between processors and peripherals.

Block Diagram



Features

- Controller for both the SDLC and HDLC (ISO 13239) transmission protocols
  - Based on the Intel 8XC152 Global Serial Channel (GSC), operating in SDLC Mode
  - Additional features support HDLC and proprietary serial protocols.
- Flexible Frame Formatting
  - Programmable preamble pattern and preamble length
  - Programmable inter-frame space
  - Single- or double-byte address field
  - Address filtering allowing multicast and broadcast
  - Raw transmit and receive testing modes
  - Back-to-back transmit & back-to back receive
  - NRZ, NRZI, Bi-Phase-S, and Manchester Data Encoding
  - Bit Stuffing and Bit Stripping
  - 16-bit (CRC-16, CCITT or IBM) and 32--bit (CRC-32) frame check sequence
  - CRC, Bit-stuffing/stripping, and abort and idle sequences detection can be independently enabled/disabled
- Flexible Serial Link Interface
  - Full or Half Duplex
  - Programmable Baud Rate
  - Modem Controls (RTSn/CTSn)
  - Collision detection
  - Internal baud generator, or external transmit clock with strobe
  - Automatic receive clock recovery, or external receive clock with strobe
- Easy to Integrate
  - Suitable for interrupt-based or polling-based operation
  - Configurable size, Transmit & Receive FIFOs
  - 80xc152-like control-status registers
  - APB or Generic MCU-like Host Interface

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Implementation Results

HSDLC core reference designs have been evaluated in a variety of technologies. The following table provides sample performance and resource utilization data. Please contact CAST to get characterization data for your target configuration and technology.

Supported Family / Device	Logic	Memory Bits	Frequency (MHz)
Cyclone-V 5CEBA9F31C7	412 ALMs	0	162
Arria-V 5AGXBB3D4F35C4	414 ALMs	0	202
Arria10 10AS057K2F35I2LG	420 ALMs	0	327
Max10 10M50DAF484C6GES	836 LEs	0	136

Verification

The HSDLC core has been verified through extensive simulation and rigorous code coverage measurements.

Deliverables

The core includes everything required for successful implementation:

- Verilog RTL source code
- Post-synthesis EDIF (netlist licenses)
- Testbenches
- Simulation scripts
- Synthesis scripts
- Documentation

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