

CAST



SPDIF-APB

Digital Audio Interface Core

Implements the Sony/Philips Digital Interface (SPDIF), a unidirectional and self-clocking interface for connecting digital audio equipment using linear PCM coded audio samples.

The SPDIF core conforms to the IEC 60958 international standard for transmitting and receiving fast audio data. This variation includes a standard bus interface to the AMBA™ APB, making it straightforward to integrate the SPDIF core with a master system for further processing of the audio data.

Data collected by the SPDIF-APB is stored in the core's internal FIFO, allowing the system to process a relatively slow audio stream in the interrupt triggered subroutines. The core could also be used for fast serial non-audio transmission.

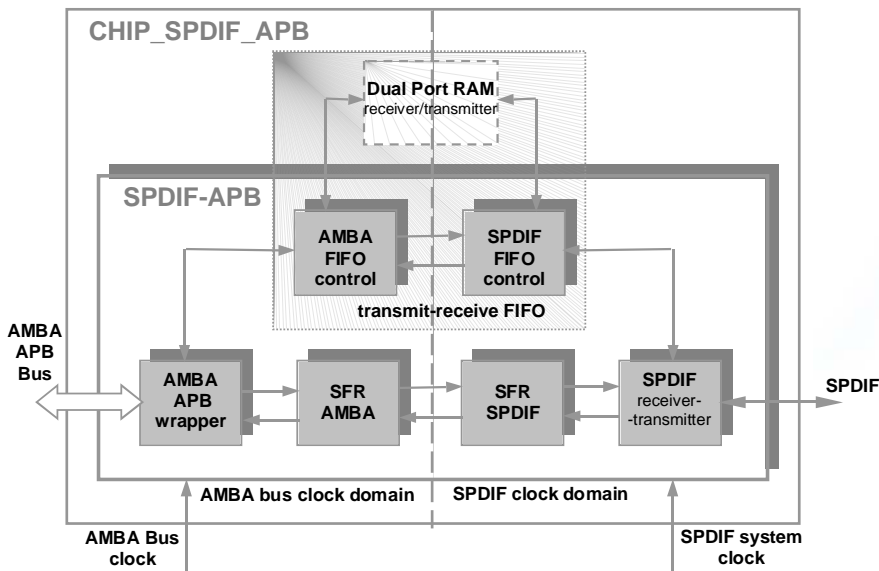
The SPDIF-APB is a microcode-free design developed for reuse in ASIC and FPGA implementations. The design is strictly synchronous with positive-edge clocking, no internal tri-states and a synchronous reset; therefore scan insertion is straightforward.

Applications

The core is suitable for implementing a unidirectional, high-speed, digital audio interface in a variety of systems, including:

- CD players
- Digital audio tape (DAT) recorders and players
- Advanced audio encoding/decoding blocks

Block Diagram



Features

- Conforms to the IEC 60958 International Standard
- Programmable: supports both Receiver and Transmitter modes
- Data mode capabilities:
 - Supports sample rates from 3kHz to 192kHz (with 98MHz SPDIF system clock)
 - 20/24 bits per sample
- Programmable transmission rate
- Programmable parity bit checking and generation
- Performs master DMA handshake interfacing
- Includes configurable internal FIFO for data streaming, with FIFO control/status signals
- Power safe capability
- Internal, event stimulated, interrupt request generation, with masking capability
- Synchronization hold in the under run condition
- Clock recovery from the SPDIF data stream
- Detection of sample rate from the received data stream
- Host processor interface:
 - AMBA APB slave unit to interface with the host APB controller, especially DMA
 - Other standard interfaces available
- Other standard processor interfaces available
- Sophisticated self-checking Test-bench (Verilog versions use Verilog 2001)

Functional Description

The SPDIF core is partitioned into modules as shown in figure above and described below. The dashed line shows the core's two clock domain areas.

AMBA APB wrapper

Compatible with AMBA APB bus specification v.2.0, and connects the SFR block and the FIFO to the AMBA APB bus.

The APB slave wrapper implements two bus slave interfaces that have separate select signals for SFR registers and for FIFO, but the other APB bus signals are shared.

SFR AHBA, SFR SPDIF

SFR is composed of two parts: SFR_AMBA belongs to the AMBA clock domain, and SFR_SPDIF belongs to the SPDIF system clock domain. The SFR_AMBA performs mandatory tasks of the SFR while SFR_SPDIF serves only for domain synchronizing.

The SFR is a set of 4 registers that provides the status of the SPDIF core and its FIFO and controls some of their settings.

The two-bit address bus *addr* addresses a particular register for read/write operation. SFR registers can be accessed only in 32-bit bus access mode.

AMBA FIFO, SPDIF FIFO

Two FIFO controllers transfer data between the core's two clock domains. All data is transferred by the synchronous dual-port RAM memory, which has two ports that are connected to the AMBA and SPDIF parts of the controller. These two clock domain parts of the FIFO controller synchronize themselves with Grey-coded index addresses.

SPDIF

Provides the digital audio interface functions according to the specification. Detailed features include: FIFO control/status signals; underrun and overrun flags; lock and syncerror flags indicating the status of synchronizing the core with the input data stream; and the ability to hold the receiver synchronized when underrun occurs.

DPRAM – Dual Port RAM Module

A technology-dependent synchronous memory module that is used to synchronize data between two clock domains and for data steaming. There is no synthesizable RTL code for the DPDRAM module in the SPDIF core deliverables.

Implementation Results

SPDIF-APB reference designs have been evaluated in a variety of technologies. The following are sample Xilinx results configured with a buffer size of 64x30 bits implemented using a DPRAM.

Xilinx Device	Slices	BRAM	I/Os	Fmax (MHz)	ISE
Spartan-3E XC3S1200E-5	526	1	82	80	12.2i
Spartan-6 XC6SLX75-3	213	1	82	120	12.2i
Virtex-5 XC5VLX110-3	357	1	82	200	12.2i
Virtex-6 XC6VLX130T-3	229	1	82	226	12.2i

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Verification

The core has been verified through extensive simulation and rigorous code coverage measurements.

Deliverables

The core includes everything required for successful implementation. The Xilinx version includes:

- Post-synthesis EDIF netlist
- An example APB slave design, which uses the SPDIF-APB in a sample system and shows how to interface with the APB
- Sophisticated self-checking Testbench (Verilog versions use Verilog 2001) including a sample chip design, external dual-port RAM for the FIFOs, a clock generator, and a set of bus functional models for APB and SPDIF buses, and a set of comparison units for monitors the correctness of data sent or received on the SPDIF bus
- A collection of test cases that covers all functionalities of the core and fulfills strict Code Coverage requirements.
- Simulation script, vectors, expected results, and comparison utility
- Place and route (firm) script
- Scan support insertion scripts
- Comprehensive user documentation, including detailed specifications and a system integration guide