

# CAST



## I2S-SC

### Inter-IC Sound Bus Controller Core

This I2C audio bus controller IP core implements an optimized, configurable, single-channel Inter-IC Sound (I2S) interface that combines both transmitter and receiver functions.

The core is compatible with the Philips I2S specification and all its modes. Instead of using eight channels, it more efficiently requires just one channel and uses time Division Multiplexing (TDM) for multi-channel communication.

A wide range of configurable transmission parameters add flexibility and allow for extending the core's functionality beyond the I2S standard. These include serial clock and word select polarities, audio channel width, data delay, the size of external FIFO, and the sample bits order. An included tool makes configuration simple.

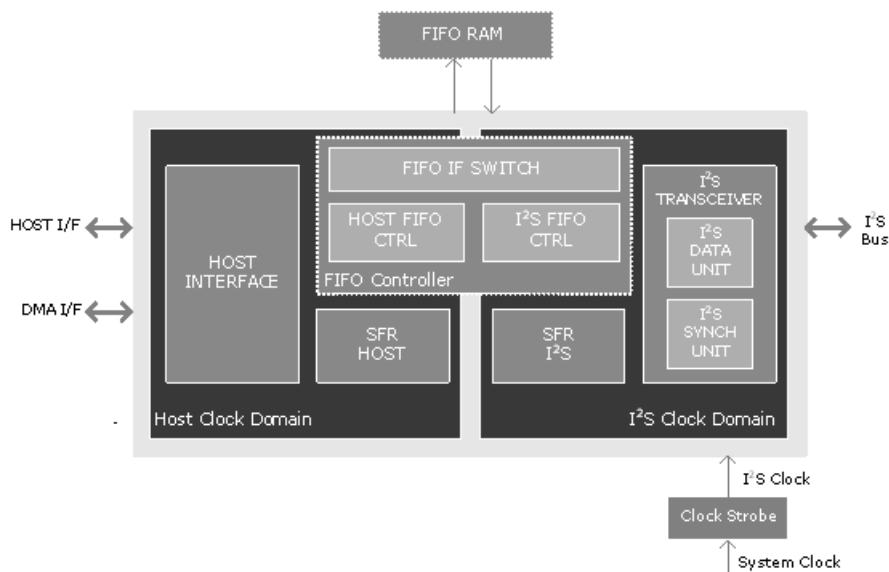
The core supports the universal OCP socket interface, with various wrappers available for other system buses, such as AMBA® AHB and APB, or CoreConnect™ PLB. The core builds on a previous version that has been successfully fabricated in ASICs and FPGAs by multiple CAST customers.

### Applications

The I2S-SC core can be used in a variety of Inter-IC Sound (I2S) bus interface controller applications, including:

- ASIC and SoC applications requiring single channel audio data transmission
- Connecting Analog to Digital and Digital to Analog converters with very low jitter
- Digital audio interface of embedded microcontroller systems
- Error correction for compact disc and digital recording
- Digital signal processing and multimedia systems in general

### Block Diagram



### Features

- Meets Philips Inter-IC Sound Bus Specification
- Supported modes
  - I<sup>2</sup>S Philips
  - Left Justified
  - Right Justified
  - DSP
  - Time Division Multiplexing (TDM)
- Two clock domains
  - Host side clock domain
  - System clock for the I2S channel
- One wide-configurable stereo channel with up to 16 optional channels with TDM support
- Set of SCK (SCLK) and WS (LRCLK) strobes
- A number of possible host-side slave interfaces for data and configuration:
  - OCP™ slave interface
  - AMBA® APB
  - AMBA® AHB
  - CoreConnect™ PLB
- Contains configurable FIFO buffer for transmission channel
- Interrupts driven by the I<sup>2</sup>S bus activity events
- Handshake interface to external DMA modules
- Extensive core configurability: choose options as needed, or use fully-configurable version
- I2S-SC consists of:
  - OCP™ compliant slave interface
  - Optional AMBA® APB, AMBA® AHB or CoreConnect™ PLB bus wrapper
  - Transmission FIFO controller
  - Special Function Registers block (SFR)
  - Single channel I<sup>2</sup>S half-duplex transceiver

### Configurability

A Design Configurator tool is available to aid in the selection of the core's many options.

## Functional Description

The I2S-SC core is partitioned into modules, as shown in the figure above and described below:

### Host Interface

The host-side slave interface connects the SFR block and the FIFO buffers to the system bus. It integrates two slave interfaces for FIFO and SFR block access. While bus signals are shared, both FIFO and SFR blocks have different addresses. These slave interfaces will be designated below as SFR system bus slave and FIFO system bus slave.

It is possible to implement one of several system bus interfaces. The base host-side interface type is the OCP™ ver.2.2 compliant slave socket, but the AMBA® AHB bus ver.2.0, AMBA® APB bus ver.2.0, or CoreConnect™ PLB slave interface can be used to connect the SFR block and the FIFO buffers to the system bus.

Since the system parallel data buses have configurable widths, the I2S-SC can be implemented into 8, 16 or 32-bit architecture systems.

### FIFO Controller

The FIFO Controller is comprised of two FIFO control units (named HOST FIFO and I2S FIFO) for each clock domain and FIFO memory interface switch module. Implementation of the FIFO memory interface switch allows use of the 1R1W block of the DPRAM as a FIFO memory for both receiver and transmitter modes. HOST FIFO and I2S FIFO control components are two FIFO buffer controllers, and together with the block of DPRAM memory and interface switch, they make the data buffer. The FIFO buffer is equipped with appropriate cross clock domain logic.

### SFR HOST, SFR I<sup>2</sup>S

The Special Function Registers block is composed of two parts: SFR HOST and SFR I2S. The former belongs to the system clock domain, while the latter belongs to the I2S system clock domain.

The SFR HOST performs mandatory tasks of SFR, while the SFR I2S provides the cross clock domain synchronization logic.

The SFR is a set of seven 32-bit registers that provides the status of the I2S core and FIFO buffers and allows for configuration of the core.

### I<sup>2</sup>S Transceiver

The single channel of the I2S transceiver block can operate as either a transmitter or receiver at once. The mode of operation for a transceiver can be set in the SFR block. There is a separate unit in the core that provides synchronization with the I2S bus.

### RAM

The transmit and receive RAM component is a dual-port synchronous RAM (1R1W) memory. The memory module has two independent ports that enable parallel access to a single

memory space. The size of the FIFO buffer can be selected by the user, and this can be set using synthesis parameters.

### Clock Synch

The Clock Synch is the clock synchronization for the I2S channel. It includes clock gating logic for the I2S transceiver. The transceiver can be turned on/off by blocking the clock signal.

## Implementation Results

I2S-SC reference designs have been evaluated in a variety of technologies. I2S-SC reference designs have been evaluated in a variety of technologies. The following are sample Xilinx results optimized for speed with an OCP interface, TDM, 32-bit data buses, and a 16-word FIFO.

Xilinx Device	Slices	BRAM	Special Features	I/Os	Fmax (MHz)	ISE
Virtex-5 XC5VLC110-2	449	1	-	93	203	11.5
Virtex-6 XC6VLX75-2	501	1	-	93	225	11.5
Spartan-6 XC6SLX75-3	507	1	-	93	125	11.5

## Support

The core, as delivered, is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, beginning with the first interaction. Additional maintenance and support options are available.

## Verification

Functional verification of the synthesizable core was performed with a VHDL/Verilog testbench. The top level testbench contains a synthesizable module of the I2S-SC core and additional environment modules such as stimulus vectors, generator, and output vectors comparator.

Formal verification was performed for OCP, AMBA AHB, and APB interfaces and wrappers.

Hardware verification of the prototype was performed with a FPGA board running a sample application.

## Deliverables

The core includes everything required for successful implementation. The Xilinx version includes:

- Post-synthesis EDIF netlist An example I2S-SC chip implementation
- Sophisticated HDL Testbench including external FIFOs, buffers, clock generators, and models of interfaces
- Simulation script, vectors, expected results, and comparison utility
- Place and route script
- Comprehensive user documentation, including detailed specifications and a system integration guide

## Related Products

**I2S** – the basic version of the I2S-SC core, which implements eight channels of the Inter-IC Sound (I2S) serial buses and combines transmitter and receiver tasks.

## Configurability

A Design Configurator tool is available to help in the selection of the core's many options. The configurable options include:

- Serial clock (SCK) polarity
- Word select (WS) polarity
- Frame synchronization / word select mode

- Audio channel width
- Data delay
- Data align within audio channel and host data bus
- Sample bit order
- Audio/mono mode
- Time Division Multiplexing (TDM) implementation
- Size of external FIFO (default value is 16 words)
- Width of data registers – maximum audio data width
- Host-side interface type
- Width of host data buses

## Example Application

The example application consists of the following IP cores:

- ATAIF – Parallel ATA controller
- I2S controller
- CPU (C68000 microprocessor)

The CPU working as the Data Processing Unit reads audio data from the CD-ROM through the ATAIF. It then writes the data to the single channel I2S-SC core. The I2S-SC core transfers these data to speakers with an I2S interface.

