

CAST

I2S-MC

Multi-Channel Inter-IC Sound Bus Core

Features

The I2S-MC core integrates eight channels of Inter-IC Sound compatible serial buses. I2S is a well-known stereo audio transmission standard, widely used to connect system elements such as Analog to Digital and Digital to Analog converters.

By using the I2S-MC module in a SoC design, a designer can easily integrate the core used for multi-channel audio transmission with the master system based on a standard AMBA APB bus for further data processing. In order to facilitate the use of the I2S core in AMBA bus based microprocessor systems, it is provided with an AMBA™ APB bus wrapper, transmit and receive FIFO control units, special function registers block (SFR), and 8-channels of the I2S core.

The data collected by the I2S-MC core is stored in the core's internal FIFO. This use of an internal FIFO allows the system to process the relatively slow audio stream in the interrupt-triggered subroutines.

The collected data can then be easily and quickly accessed by the master system by the AMBA APB bus by any APB bus master.

Developed for reuse in ASIC and FPGA implementations, the design is strictly synchronous with two clock domains, positive-edge clocking in both domains (except for four flip-flops for reset signal synchronization). There are no internal tri-states and asynchronous resets, therefore scan insertion is straightforward.

- Meets Philips Inter-IC Sound Bus Specification
- Supported modes
 - I2S Philips
 - Left Justified
 - Right Justified
 - DSP
- Two clock domains
 - APB the host side clock domain
 - system clock for the I2S channels
- Eight configurable stereo channels
- Two sets of SCK (SCLK) and WS (LRCLK) strobes
 - one for all transmitters
 - one for all receivers
- AMBA™ APB bus slave interface for data and configuration
- Contains two configurable FIFO buffers
 - one for all transmit channels
 - one for all receive channels
- One configuration register block for all channels
- Interrupts driven by the I2S bus activity events
- Handshake interface to external DMA modules
- Sophisticated self-checking Testbench (Verilog versions use Verilog 2001)

Applications

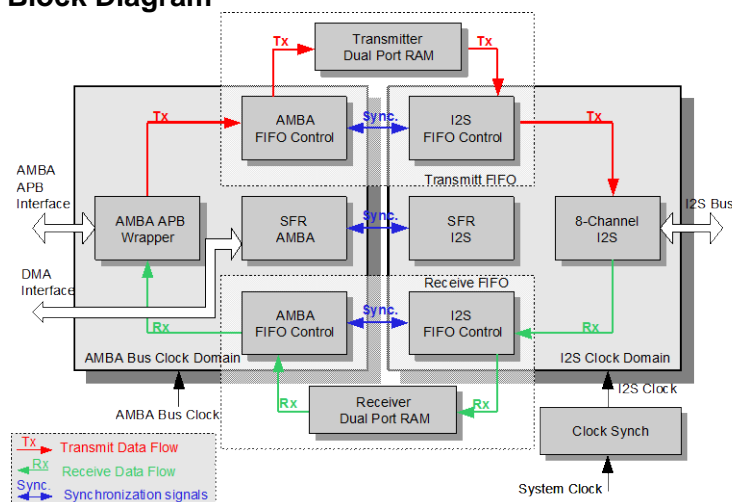
The I2S-MC can be utilized for a variety of Inter-IC Sound compatible serial bus applications including:

- ASIC and SoC applications requiring up to 8 channel audio data transmission
- Connecting Analog to Digital and Digital to Analog converters with very low jitter
- Digital audio interface of embedded microcontroller systems
- Error correction for compact disc and digital recording
- Digital signal processing and multimedia systems in general

Configurability

- Synthesis parameters allow adjustment to the target application

Block Diagram



Functional Description

The I2S-MC core is partitioned into modules as shown in block diagram above.

AMBA APB Wrapper

The APB bus slave wrapper, which is compatible with AMBA™ APB bus specification v.2.0, connects the SFR block and the FIFO buffers to the AMBA™ APB bus. The APB bus slave wrapper implements two APB bus slave interfaces that have separate select signals *pselsfr* and *pselfifo*, but share other bus signals. These slave interfaces will be henceforth denoted as APB SFR bus slave and APB FIFO bus slave.

8-Channel I2S

Each of the 8-channels of the I2S block can operate as either a transmitter or receiver. The mode of operation for a given channel can be set in the SFR block. There are two units in the core that provide synchronization with the I2S bus for all channels. One of them provides synchronizing signals for all transmitters while another one provides synchronizing signals for all receivers.

The I2S Bus controller may operate in one of the following modes:

- Master Transmitter Mode: serial data is transmitted through SD while SCK and WS output serial clock and word select, respectively.
- Slave Transmitter Mode: serial data is transmitted via SD while serial clock and word select are input through SCK and WS, respectively.
- Slave Receiver Mode: serial data, serial clock and word select are received through SD, SCK and WS, respectively.
- Master Receiver Mode: serial data is received via SD while SCK and WS output serial clock and word select, respectively.

The I2S Bus Interface may operate in one of the following four configurations:

- I2S – Philips mode
- Let Justified mode (also known as DSP)
- Right Justified mode
- DSP mode

Every mode can be fixed by the set of synthesis parameters and cannot be changed after synthesis, but it is also available to set one of these modes to be a default mode and it can be still configurable by software.

SFR AMBA, SFR I2S

The Special Function Registers block is composed of two parts: SFR AMBA and SFR I2S. The former one belongs to the AMBA clock domain while the latter belongs to the I2S system clock domain. The SFR AMBA performs mandatory tasks of SFR while the SFR I2S provides the cross clock domain synchronization logic.

- The SFR is a set of nine 32bit registers that provides status of the I2S core and FIFO buffers and allows for configuration of the core. To address particular register for read/write operation three bit address bus is used. The SFR registers can be accessed only in the 32bit bus access mode.

AMBA FIFO Control, I2S FIFO Control

The AMBA FIFO Control and I2S FIFO Control components are two FIFO buffer controllers, together with two blocks of the DPRAM (1r1w) memory they make the data buffers. Both FIFO buffers are equipped with appropriate cross clock domain logic.

Transmitter and Receiver Dual Port RAM

The transmit RAM and Receive RAM component is a dual-port synchronous RAM (1r1w) memory. The memory module has two independent ports that enable parallel access to a single memory space, the size of the FIFO buffers can be chosen by the user, it can be set using synthesis parameters.

Clock Synch

The Clock Synch – is the clock synchronization for I2S channels. It includes clock gating logic for all channels. Each channel can be individually turned on/off by blocking clock signal for this channel. The clock signal can be blocked also for transmit or receive synchronization unit.

Implementation Results

I2S-MC reference designs have been evaluated in a variety of technologies. The following are sample ASIC results were implemented without FIFO buffers memory and were optimized for speed.

ASIC Technology	Approx. Area	Frequency	
		pclk	clk
TSMC Artisan 0.13 um	24,400 gates	68 MHz	85 MHz
TSMC Artisan 0.09 um	23,900 gates	104 MHz	119 MHz

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Verification

Functional verification of synthesizable core is performed with a Verilog testbench. The top level of testbench contains synthesizable block of I2S-MC core and additional environment modules like stimulus vectors generator and output vectors comparator.

Hardware verification of the prototype was realized with the aid of application demo. This application was developed on proprietary EB-3 Demo Board.

Deliverables

The core includes everything required for successful implementation. The ASIC version includes:

- Verilog 2001 RTL source code
- Example design for I2S-MC (CHIP_I2S_MC)
- Sophisticated Verilog 2001 self-checking Testbench
- Simulation script, vectors, and expected results
- Synthesis script
- Comprehensive user documentation, including detailed specifications and a system integration guide