

CAST

T8051

Tiny 8051-Compatible Microcontroller Core

A semiconductor IP core that implements an extremely small 8-bit microcontroller executing the ASM51 instruction set. It includes peripherals for serial communication, a timer, a multi-purpose I/O port, hardware interrupts, and a JTAG debugger interface.

This 8051 core is based on the fast, configurable CAST R8051XC2 core (proven in hundreds of successful designs). Sample implementation results show it to require as little as 2,000 ASIC gates for 0.35 μm (for the CPU). It achieves this low gate count by sharing resources between several stages of instruction set execution, with careful tuning of instruction cycle latency to reduce hardware resources.

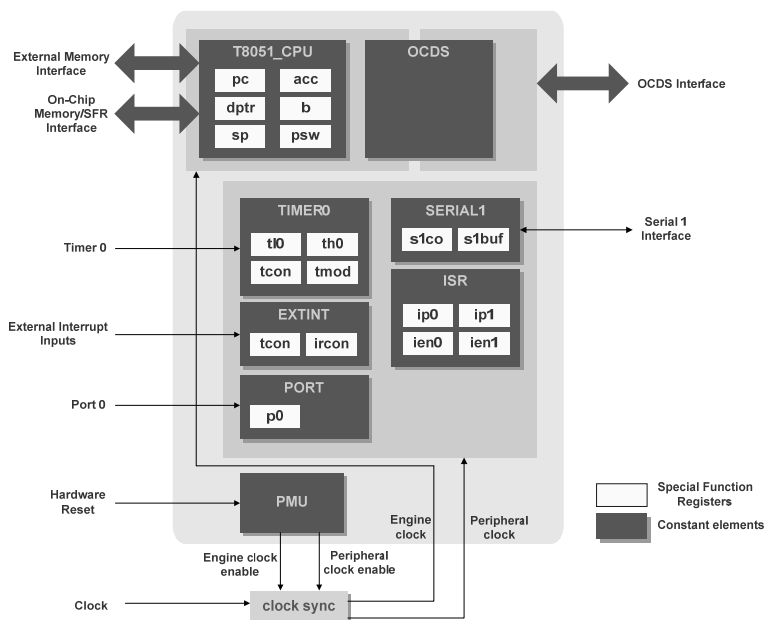
Performance remains high: 4.1 times better than the original Intel™ 8051 as measured by Dhrystone MIPS per MHz. Communication with both built-in and external memories has been accelerated by de-multiplexing the address and data buses, while alternate port functions such as external interrupts and serial interface are available on separate pins.

The T8051 is a microcode-free design developed for reuse in ASIC and FPGA implementations. The design is strictly synchronous with positive-edge clocking (except in the optional debug module), no internal tri-states and a synchronous reset; therefore scan insertion is straightforward. A complete On-Chip Debug Support (OCDS) debugging system compatible with the industry-standard Keil™ μVision Cx51 Development Tools IDE is also available.

Applications

This small 8051 microcontroller core is ideal for silicon space-challenged mixed-signal systems (e.g., Zigbee products). It also provides an easily-programmed alternative to hard-coded control logic in many existing applications, and is an excellent choice for low-power and small FPGA-based systems.

Block Diagram



Features

- 100% MCS51® compliant Central Processing Unit
- Extremely small gate count, e.g., TSMC .18 ASIC process: CPU only = 2.8K
CPU + peripherals = 5.2K (fits in 0.0539 mm² footprint)
Total, with OCDS debug = 8.5K
- Dummy peripheral replacements for even lower gate count
- Low power consumption
- Fast: performance is 4.1 times classic 8051 (Dhrystone MIPS benchmarks; data available).
- Input/Output port
 - Single 8-bit I/O port
 - Alternate port functions such as external interrupts and serial interface are separated, providing extra port pins when compared with the standard 8051
- 16-bit Timers/Counter
 - 80C51-like Timer 0
- Full Duplex Serial Interface
 - Serial 1 (80517-like)
 - 8-bit UART mode, variable baud rate
 - 9-bit UART mode, variable baud rate
 - Baud Rate Generator
- Interrupt Controller
 - Four Priority Levels with eleven interrupt sources (80C517-like)
 - Eight External Interrupts
 - Two Low-Level or Falling-Edge Sensitive
 - Two Falling-Edge or Rising-Edge Sensitive
 - Four Rising-Edge Sensitive
- Internal Data Memory interface
 - addresses up to 256 B of Data Memory Space
- External Memory interface
 - addresses up to 64 kB of External Program Memory
 - addresses up to 64 kB of External Data Memory
 - De-multiplexed Address/Data Bus to ease the connection with memories
 - Program memory write mode
- On-Chip Special Function Registers interface
- Power Management Unit
- On Chip Debug Support (OCDS)

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Functional Description

The T8051 core is partitioned into modules as shown in the block diagram and described below.

T8051 CPU – Central Processing Unit

Fetches instructions from program memory and uses RAM or SFRs as operands. It provides the ALU with 8-bit arithmetic, logic, multiplication and division operations as well as Boolean manipulations. The RAM and SFR interfaces can address up to 256 bytes of Read/Write Data Memory Space and built-in or off-core Special Function Registers. The memory interface can address up to 64kB of both Program Memory and External Data Memory.

Port

A parallel I/O port controller serves the parallel 8-bit I/O port for off-core buffers, and is classic 80C51-compatible.

Serial1

The core includes a flexible UART (Universal Asynchronous Receiver/Transmitter) port for full-duplex communication. The Serial1 port operates in 8- or 9-bit UART mode; the variable baud rate is generated internally.

Extint

Eight external interrupt inputs are sampled and edge/level checked in this module. Two interrupts are falling-edge or low-level sensitive, two are rising- or falling-edge, and the remaining four are rising-edge sensitive.

Timer0

Provides four modes of operation: 13-bit timer/counter, 16-bit timer/counter, 8-bit timer/counter with auto reload, and dual 8-bit timer. Can count external pulses (1 to 0 transitions) on the corresponding “t0” pin. Gating the timer/counter using an external control signal, allows it to measure the pulse width of external signals.

ISR - Interrupt Service Routine

The core has an 80C51-compatible Interrupt Controller with eleven sources and four priority levels. Each source has its own request flag(s) located in a dedicated SFR. Each interrupt requested by the corresponding flag can be individually enabled or disabled by dedicated enable bits in the SFRs.

PMU - Power Management Unit

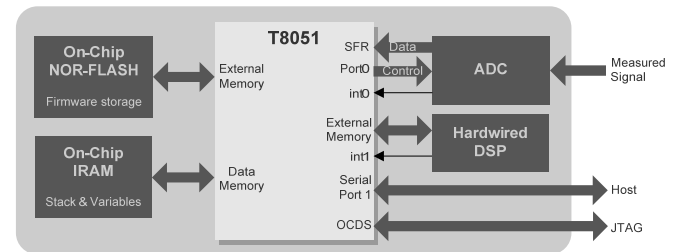
Serves two power management modes: IDLE and STOP. The IDLE mode leaves the clock for peripherals running; power consumption drops because the CPU is not active. The CPU can exit IDLE state with any interrupt or reset. In the STOP Mode, all internal clocks are turned off. The CPU will exit this state with a non-clocked external interrupt (i.e. one of two, level-triggered interrupts) or a reset condition.

OCDS - On Chip Debug Support

Serves as a debug interface through an IEEE1149.1 (JTAG) port. The OCDS unit provides the following functions: Run, Stop, Single-step, hardware and software breakpoints, debugger program execution and Read/Write Access to Program Memory, External/Internal Data Memory and SFRs.

Example Application

Here the T8051 microcontroller serves as an industrial meter (e.g. to measure energy or rotation).



The Analog/Digital Converter (ADC) controlled through the core's Special Function Registers (SFR) interface provides measured data that is processed first by the CPU, then by the custom-designed DSP block with high-precision arithmetic. The data is stored back in the on-chip RAM, and can be read by the external host using the core's UART (Serial Port 1) interface. The included JTAG-accessible OCDS facilitates firmware (algorithm) development, debugging, and modifications, and also works for production programming of the on-chip NOR-FLASH memory.

Implementation Results

T8051 reference designs have been evaluated in a variety of technologies. The following are sample results using optimization for area. The Area figures show the total (CPU, peripherals, and OCDS debug), CPU only, and size of the optional OCDS.

ASIC Technology	Area			Speed
	Total	CPU Only	Opt. OCDS	
TSMC* 0.35µm	0.4730mm ² , 6.8k gates	2.2k gates	2.5k gates	45 MHz
UMC 0.25µm	0.2096mm ² , 8.8k gates	3.2k gates	3.5k gates	85 MHz
UMC 0.18µm	0.1084mm ² , 8.9k gates	3k gates	3.2k gates	130 MHz
TSMC* 0.18µm	0.0849mm ² , 8.5k gates	2.8k gates	3.1k gates	115 MHz
UMC 0.13µm	0.0477mm ² , 9.2k gates	3.3k gates	3.8k gates	155 MHz
TSMC* 0.13µm	0.0429mm ² , 8.4k gates	2.8k gates	3.1k gates	133 MHz
TSMC* 0.09µm	0.0236mm ² , 8.4k gates	2.7k gates	3k gates	233 MHz
UMC 0.065µm	0.0127mm ² , 8.9k gates	2.9k gates	3.2k gates	450 MHz

* Artisan TSMC library

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Verification

The core has been verified through extensive simulation and rigorous code coverage measurements. All subcomponents were functionally verified with an HDL testbench using their individual test suites. The CPU and ALU have been verified against a proprietary hardware modeler and behavioral models. The test suite for the peripherals has also been developed in their own testbenches, based on either hardware or behavioral models.

The trial ATPG coverage figures met the requirements and reached level of 99%. Additionally the value of IDDQ reached level of 99%.

Deliverables

The core includes everything required for successful implementation:

- HDL RTL source code (soft core) or a post-synthesis EDIF netlist (firm core)
- Reference design for proprietary development board
This design uses the T8051 and illustrates how to build and connect memories and port modules
- Sophisticated HDL Testbench including external FIFOs, buffers, models of interfaces, and the core
- Simulation script, vectors, expected results, and comparison utility
- Synthesis (soft) or place and route (firm) script
- Comprehensive user documentation, including detailed specifications and a system integration guide