

CAST

R8051XC2

High-Performance,
Configurable, 8-bit
Microcontroller Core

The R8051XC2 configurable processor core implements a range of fast, 8-bit, micro-controllers that execute the MCS@51 instruction set.

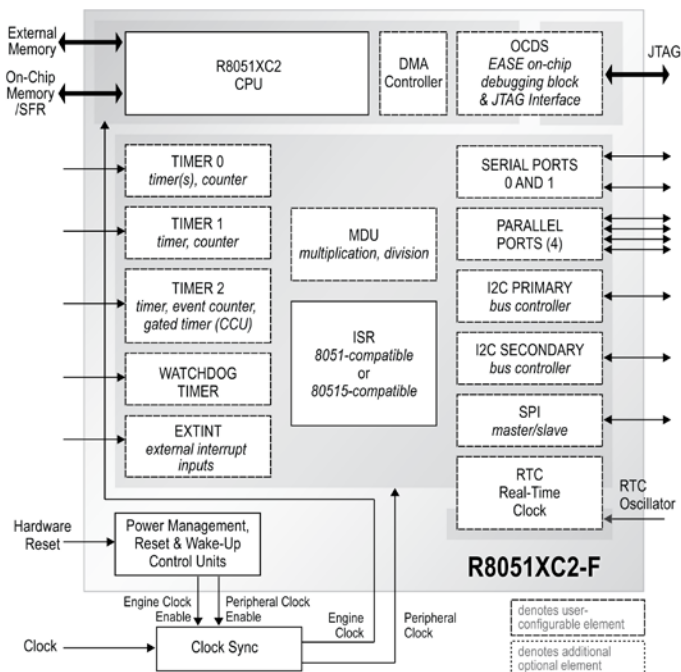
The IP core runs with a single clock per machine cycle, and requires an average of 2.12 machine cycles per instruction. Dhrystone 2.1 tests show it to run from 9.4 to 12.1 times faster than the original 8051 at the same frequency. Representative 90 nm ASIC results have reached 430 MHz, for an effective speed-up of 400 times over 80C51 chips.

The core has a rich set of optional features and peripherals. Designers can choose from several versions, including the easy-to-configure full version with all options included; a custom, non-configurable version with options specified at purchase; and pre-packaged versions with different sets of options and degrees of configurability.

All versions of the core benefit from power-saving architectural efficiency—the R8051XC2 is 10% better in milliwatts/DMIP than our previous generation—and various power-management options are available. System development is facilitated through the EASE native on-chip debugging option and support by Keil's C51 integrated development environment.

This new product builds on CAST's experience with hundreds of 8051 IP customers going back to 1997. Designed for easy reuse in ASICs, structured ASICs, or FPGAs, the core is strictly synchronous, with positive-edge clocking (except in the optional debug & SPI modules), synchronous reset, and no internal tri-states. Representative 90nm ASIC results show the core to be conservative in its use of space, requiring just 8,000 to 71,000 gates.

Block Diagram



Features

- Fully compatible with the MCS@51 instruction set
- Single clock per cycle and efficient architecture for up to 12.1 times the performance of original 8051
- Fewer machine cycles means lower average power usage in most applications
- Extensive set of optional features and peripherals: choose configurable or less-expensive fixed versions
- EASE Debugging option: On-Chip Debug Support (OCDS) block that interfaces through IEEE1149.1 (JTAG) port; external debugging pod with JTAG and USB; and debugging software with interface to Keil C51 tools

Options and Peripherals

Full user-configurable version includes all of these; other versions include a subset (see Versions).

External Memory Interface:

- Addresses up to 8 MB of Program and Data Memory each (when using memory banking)
- One, two or eight Data Pointers for fast data block transfer
- Additional Arithmetic Unit supports data pointers, auto-increment/-decrement, and auto-switch
- Supports external DMA controller through HOLD function
- Program memory write mode

Direct Memory Access (DMA) Controller:

- Up to eight independent channels
- Read/Write Access to all memory spaces (incl. SFR)
- Linear addressing (up to 8MB)
- Address auto-increment/decrement
- Synchronous/asynchronous Mode
- Software/Hardware Triggers

Multiplication-Division Unit:

- 16 x 16-bit multiplication,
- 32/16- and 16/16-bit division,
- 32-bit normalization and L/R shifting

Special Function Registers Interface: services from 43 to 119 external SFRs

Features continue >

Features (continued)

Interrupt Controller:

- Four priority levels with eighteen interrupt sources, or
- Two priority levels with six sources

Input/Output Interfaces

- Parallel Ports: up to four 8-bit Input/Output ports
- Serial 0 interface:
 - Full-duplex serial interface (80C51-like),
 - Equipped with an additional baud rate generator
- Serial 1 interface:
an asynchronous-only version of Serial 0

- SPI Master/Slave interface
- I2C™ Master/Slave interfaces: one or two

Timers and Counters

- 16-bit Timers/Counters:
 - Timers 0 and 1: 80C51-like simple timers
 - Timer 2: 80C51-like, operates as timer, event counter or gated timer
- Watchdog Timer: 15-bit programmable

Power Management Unit with power-down modes (IDLE/STOP)

Verification: all versions include sophisticated self-checking Testbench (Verilog versions use Verilog 2001) with CPU behavioral model, memory models, and more

Applications

The 8051 continues to be a rigorous and cost-effective solution for many applications, and the fast, flexible R8051XC2 is an especially good choice for many systems. Popular uses include data management control for complex systems, and interface control for analog and sensing chips.

Functional Description

The core is partitioned into modules as shown in the block diagram and described below.

CPU: Central Processing Unit

Fetches instructions from program memory and uses RAM or SFRs as operands. Provides the ALU for 8-bit arithmetic, logic, multiplication and division operations, and Boolean manipulations. The RAM and SFR interface can address up to 256 bytes of Read/Write Data Memory Space and built-in and off-core Special Function Registers. The memory interface can address from 64KB to 8MB of Program Memory, and from 64KB up to 8MB of External Data Memory. It uses a HOLD interface to support any external DMA controller, and it eases the connection to memories using a de-multiplexed address/data bus. The variable-length code fetch and MOV_C to access fast or slow program memory—and similarly a variable-length MOV_X to access fast or slow RAM or peripherals—are provided.

DMA: Direct Memory Access Controller

Contains up to eight individual channels, each capable of transferring data from or to any addressable location (program memory, internal or external data memory, or SFR). Each channel can work in synchronous mode (when just one byte is transferred at each trigger) or asynchronous mode (when all the data is transferred at each trigger). Transfers can be triggered by software or by specified interrupt source.

MDU: Multiplication Division Unit

This on-chip arithmetic unit performs these unsigned integer operations: 16 x 16 bit multiplication; 32/16 and 16/16 bit division; and 32 bit normalization and L/R shifting

The MDU allows operations to occur concurrently to and independent of the engine activity.

Parallel Ports

Controller serves up to four parallel 8-bit I/O ports to be used with off-core buffers. It is compatible with the classic 80C51, but lacks the multiplexed memory bus feature and alternate functions. (These could be combined off-core if required).

Serial Ports 0 and 1

Two fully independent serial ports for simultaneous communication over two channels. They can operate in identical or different modes and at different communication speeds. Serial Port 0 is capable of both synchronous and asynchronous transmission, while Serial 1 provides asynchronous mode only.

In synchronous mode, the microcontroller generates a clock and operates in half-duplex mode. In asynchronous mode it can operate in full-duplex mode. Received data is buffered in a holding register, which allows the serial ports to receive an incoming word before the software has read the previous value.

Serial Port 0 offers three communication protocols: Synchronous mode, with fixed baud rate; 8-bit UART mode, with variable baud rate; and 9-bit UART mode, with variable or fixed baud rate. Serial Port 1 has two operating modes: 8- and 9-bit UART mode, with variable baud rate. Both Serial Ports include an additional Baud Rate Generator.

I2C™ Interfaces: Primary and Secondary

The primary (I2C) and secondary (SEC_I2C) I2C Bus Controllers each provide a serial interface that meets the Philips I2C bus specification v1.0 and support all master/slave receiver/transmitter modes. Each is a true multi-master bus controller, including collision detection and arbitration to prevent data corruption if two or more masters simultaneously initiate data transfer. They perform 8-bit oriented, bi-directional data transfers up to 100 Kbit/s in the standard mode, or up to 400 Kbit/s in the fast mode

Serial Peripheral Interface (SPI) Interface

Provides full-duplex, synchronous communication between the core and other peripheral devices, including other MCUs. It can operate either as Master or Slave, with programmable clock rate, phase, and polarity. The maximum data rate is ¼

of the system clock for a Slave, and ½ of the system clock for a Master. Write collision and overrun detection protect data, and Master mode fault detection for multi-master systems prevents bus conflict.

Timers 0 and 1

Each have these three modes: 13-bit timer/counter, 16-bit timer/counter, and 8-bit timer/counter with auto reload. Timer 0 has an additional mode: two 8-bit timers. Each timer can also count external pulses (1 to 0 transition) on the corresponding t0 or t1 pin. Another option is to gate the timer/counter using an external control signal, which allows it to measure the pulse width of external signals.

Timer 2

Operates as a timer, event counter, or gated timer.

In timer mode, it can be incremented every 12 or 24 clock cycles, depending on the prescaler setting. In event counter mode, it is incremented when an external signal changes from 1 to 0 (sampled every machine cycle). Timer 2 is incremented in the cycle following the one in which that transition was detected. In gated timer mode, its incrementing is gated by an external signal.

A Timer 2 reload can be executed in two modes. In Mode 0, the reload signal is generated by a Timer 2 overflow (auto reload), while in Mode 1 it is generated by a negative transition at the corresponding input pin t2ex.

Compare-Capture Unit

The CCU within Timer2 performs Compare and Capture functions. For the Compare function, values stored in four 16-bit compare/capture registers are compared with the contents of the Timer 2 register. The results are signaled on the “ccu-bus” outputs and interrupts are generated.

For the Capture function actual timer/counter contents can be saved into one of four 16-bit registers upon an external event (Mode 0) or software write operation (Mode 1).

Watchdog Timer

A 15-bit counter that is incremented every 24 or 384 clock cycles. After an external reset, it is disabled and all registers are set to zeros. It can be started by applying an active input during reset (hardware automatic start) or by setting the enable bit by software. Once started, it cannot be stopped unless the external reset signal becomes active.

When the Watchdog enters the state of 7CFFh, it activates a dedicated flag and forces internal reset. It can be avoided by refreshing the Watchdog with software before it reaches 7CFFh.

Power Management, Reset Control, and Wake-Up Control Units

Generates clock enable signals for the main CPU and for peripherals; serves Power Down Modes IDLE and STOP; and generates an internal synchronous reset signal (upon external reset, watchdog timer overflow or software reset condition).

The IDLE mode leaves the clock of the internal peripherals running. Power consumption drops because the CPU is not active. Any interrupt or reset will wake the CPU.

The STOP mode turns off all internal clocks. The CPU will exit this state with an external interrupt or reset. Internally generated interrupts (timer, serial port, watchdog, ...) are disabled since they require clock activity.

The Wake-up From Power-Down Mode Control Unit services two external interrupts during power-down modes. They can combinationally force the clock enable outputs back to active state so the clock generation can be resumed.

RTC: Real Time Clock

Provides a real-time count with a resolution of 1/256th second and range of 179 years. It can set and read seconds, minutes, hours, day of the week, and the date, represented by a 16-bit number interpreted by software. An alarm function can generate interrupts periodically or at a specific time, and these may be used to wake up from IDLE/STOP mode.

SFRMUX: Special Function Register Multiplexer

Provides a common bus multiplexer for all the internal and external Special Function Registers.

ISR: Interrupt Service Routine Unit

The R8051XC2 provides two types of interrupt controllers: an 8051-compatible with up to six interrupt sources and two priority levels, or an 80515-compatible with up to eighteen interrupt sources and four priority levels. Each source has its own request flag(s) located in a dedicated SFR. Each interrupt requested by the corresponding flag can be individually enabled or disabled by dedicated enable bits in the SFRs.

OCDS

Internal block and JTAG port interface for the optional EASE debugging system. It provides the following functions: Run, Stop, Single-step; Software breakpoint; Debugger program execution; Hardware breakpoints; Read/Write Access to Program Memory, External/Internal Data Memory and SFRs; and Program Trace and Data Trace (optional).

Implementation Results and Performance

The core's architecture eliminates redundant bus states and implements parallel processing of fetch and execution phases. Since a cycle is aligned with memory fetch when possible, most of the 1-byte instructions are performed in a single cycle.

The core uses one clock per cycle. This, together with other extensions (mutli-DPTR, MDU), leads to significant performance improvements with respect to the original Intel device operating with the same clock frequency.

Implementation Results and Performance, cont.

The Dhrystone 2.1 benchmark score varies from 0.088 to 0.114 DMIPS/MHz, which translates to speed improvements from 9.4 to 12.1 times over the standard 80C51, or 400 times the maximum performance at 430 MHz in 90nm technology.

Sample Dhrystone 2.1 benchmark results are as follows.

Configuration	DMIPS/MHz	80C51 Speed Ratio
Basic	0.0883	9.4
Multiple DPTR	0.1020	10.9
Multiple DPTR+auto-inc	0.1111	11.8
MDU+Multiple DPTR+auto-inc	0.1136	12.1

Reference designs have been evaluated in a variety of technologies. The following are sample results using a 90nm ASIC technology, and separate optimizations for speed and area. The EASE debug option is not included.

Version & Configuration	Maximum Speed	Minimum Area
R8051XC2 CPU	450 MHz	8.0k gates
R8051XC2-AF	435 MHz	12.5k gates
R8051XC2-BF	433 MHz	18.8k gates
R8051XC2	270 MHz	70.7k gates

Available Versions

Six versions of the core are available, offering a range of capabilities and prices.

- **R8051XC2** includes all options, and is user-configurable (i.e., options may be included or excluded prior to synthesis).
- **R8051XC2-C** includes a custom set of options specified by the customer, and is not user-configurable.
- **R8051XC2-A** includes options that match the original Intel 8051 peripheral set: 64kB memory interface, two timers, one serial port, four parallel I/O Ports, two-level interrupt controller, and two DPTR registers. These options are user-configurable (i.e., may be deleted prior to synthesis).
- **R8051XC2-AF** includes the same 8051-like set of options, but is fixed and not user-configurable.
- **R8051XC2-B** includes options that match the Infineon 80515/80517 peripheral set: 64kB memory interface, three timers, two serial ports, four parallel I/O ports, watchdog timer, multiplication-division unit, and two DPTR registers. These options are user-configurable (i.e., may be deleted prior to synthesis).
- **R8051XC2-BF** includes the same 80515/80517-like set of options, but is fixed and not user-configurable.

ASIC (RTL) and FPGA (netlist) deliverables are available; FPGA packages are not user-configurable.

The native EASE debugging package is an extra option for all versions.

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available; contact CAST Sales.

Verification

The core has been verified through extensive simulation and rigorous code coverage measurements. All subcomponents were functionally verified with an HDL testbench using their individual test suites. The CPU and ALU have been verified against a proprietary hardware modeler and behavioral models. The peripherals have also been verified in their own testbenches, based on either hardware or behavioral models. An extensive constrained random verification was performed to verify the CPU, DMA and OCDS.

Deliverables

The core is available in ASIC (synthesizable HDL) or FPGA (netlist) forms, and includes everything required for successful implementation. ASIC versions include:

- HDL RTL source code
- Easy-to-use configuration tool (with configurable versions)
- An example chip implementation, which uses the core in a sample system
- Sophisticated self-checking HDL Testbench including everything needed to test the core (Verilog versions use Verilog 2001)
- Simulation script, vectors, and expected results
- Synthesis script
- Comprehensive user documentation, including detailed specifications and a system integration guide

A reference design board is available; contact CAST Sales for information.