

CAST

R8051XC-EP

8051-Compatible Microcontroller Core

An economical, entry-point, fixed-configuration core that implements an 8051-like 8-bit microcontroller that executes all ASM51 instructions. It has the same instruction set as the 80C31, but executes operations an average of eight times faster.

The R8051XC-EP provides hardware and software interrupts, an interface for serial communication, two timers, an Intel-compatible interrupt scheme, parallel I/O ports, and a power management unit.

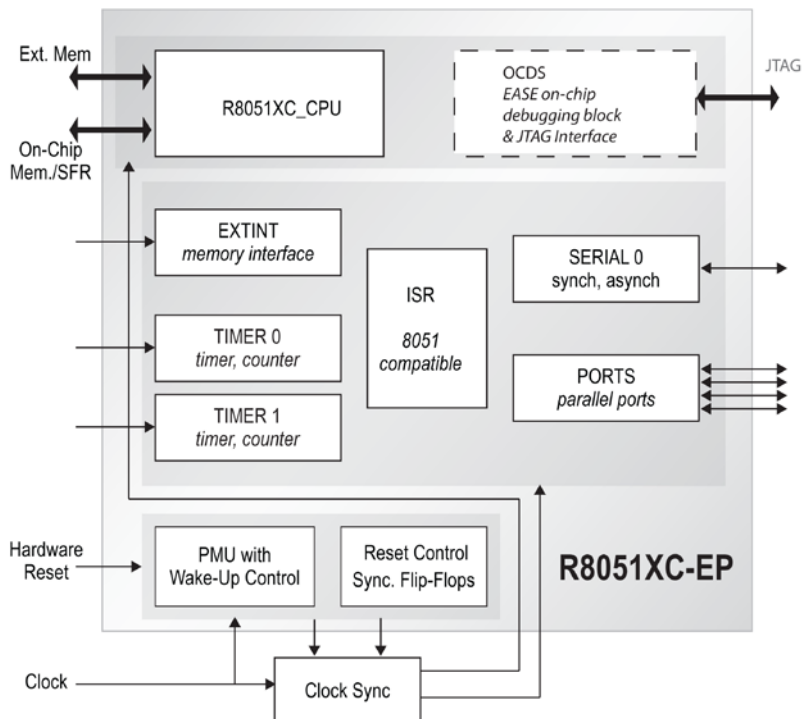
The R8051XC-EP is one of our proven 8051 family of processor cores, which have been successfully implemented in a hundred different customer products. Representative ASIC implementation data shows it to offer competitive performance and area results, requiring for example about 9,000 gates for 350 MHz.

Developed for easy reuse in ASIC and FPGA implementations, the microcode-free design is strictly synchronous, with positive-edge clocking, no internal tri-states, and a synchronous reset. Scan insertion is straightforward. System development is facilitated through the EASE native on-chip debugging option and support by Keil's C51 integrated development environment.

Applications

The R051XC-EP is suitable as a primary or secondary controller in a wide variety of applications, including 8-bit data processing systems, mobile and other products requiring low power consumption, high-speed control systems, and mixed-signal SoC applications.

Block Diagram



Features

- Control Unit
 - Eight-bit instruction decoder for MCS[®] 51 instruction set
 - Executes instructions with one clock per cycle (versus twelve for standard 80C51) for an average 8x speed up
- ALU performs 8-bit arithmetic, multiplication and division, and Boolean manipulations
- 32-bit Input/Output ports
 - Four 8-bit I/O ports
 - Alternate port functions such as external interrupts and serial interface are separated, providing extra port pins when compared with the standard 8051
- Two 16-bit Timer/Counters
- Interrupt Controller with two priority levels and five sources
- Internal Data Memory Interface can address up to 256 bytes of Read/Write Data Memory Space
- External Memory interface
 - Can address up to 8 MB of External Program Memory and up to 8 MB of External Data Memory (when using memory banking)
 - De-multiplexed Address/Data Bus for easy connection to memories
 - Variable length MOVX to access fast/slow RAM or peripherals
 - Wait cycles to access fast/slow ROM
 - Dual data pointer register
 - Program memory write mode
- Special Function Registers interface services up to 103 External SFRs
- Power Management Unit – IDLE and STOP modes
- Sophisticated self-checking Testbench (Verilog versions use Verilog 2001)
- EASE Debugging option: On-Chip Debug Support (OCDS) block that interfaces through IEEE1149.1 (JTAG) port; external debugging pod with JTAG and USB; and debugging software with interface to Keil C51 tools

Functional Description

The core is partitioned into modules as shown in the block diagram and described below.

Central Processing Unit

Fetches instructions from program memory and uses RAM or SFRs as operands. Provides the ALU for 8-bit arithmetic, logic, multiplication and division operations and Boolean manipulations. The RAM and SFR interface can address up to 256 bytes of Read/Write Data Memory Space and built-in and off-core Special Function Registers. The memory interface can address from 64K to 8M bytes of Program Memory and of Data Memory when memory banking is used.

Ports

Ports p0 – p3 are Special Function Registers that can be observed on the corresponding pins. Writing a “1” makes the corresponding pin high (VCC), and a “0” makes it low (GND). Each port is bidirectional, and consists of a Latch (SFR “p0” to “p3”), an output driver, and an input buffer. This means the CPU can output or read data through any of these ports unless a port is used for an alternate purpose.

Timers 0 and 1

Each of these two 16-bit registers can be configured as a timer or a counter. A timer is incremented every machine cycle, meaning it counts up after every 12 oscillator periods. A counter is incremented when a falling edge is recognized at a pin. Since it takes two machine cycles, the maximum input count rate is 1/24 of the oscillator frequency. There are no restrictions on the duty cycle, but to ensure proper 0 or 1 state recognition an input should be stable for at least one machine cycle.

Four operating modes are available for timers 0 and 1, selectable through two SFRs.

Serial 0

The serial buffer consists of two separate registers, a transmit buffer and receive buffer, and it can simultaneously transmit and receive data. It can also buffer one byte of received data, preventing the received data from being lost if the CPU reads the first byte before transmission of the second byte is finished. The serial port can operate in four modes, as listed in the Features.

Clock Control & Power Management Unit (PMU)

The Clock Control generates an internal synchronous reset, and contains registers for selecting clock timers. The PMU serves two power management modes, IDLE and STOP.

IDLE mode leaves the internal clock and peripherals running. Power consumption drops because the CPU is not active. Any interrupt or reset will wake the CPU. STOP mode turns off all internal clocks. The CPU will exit this state with an external interrupt or reset. Internally generated interrupts (timer, serial port, watchdog, ...) are disabled since they require clock activity.

Interrupt Service Routine Unit

The core provides five interrupt sources. Two external interrupts are edge- or level-sensitive. Two internal interrupts are associated with Timer 0 and Timer 1; the third with the Serial Port.

Implementation Results

R8051XC-EP reference designs have been evaluated in a variety of technologies. The following results use typical conditions, exclude memories, and were optimized for the clock speeds shown.

ASIC Technology	Cell Area	NAND2 Area	Approx. Area	Frequency
TSMC 0.09μ	25,439	2.8224	9,013 gates	350 MHz
TSMC 0.13μ	50,338	5.0922	9,885 gates	300 MHz
TSMC 0.18μ	101,262	9.9792	10,147 gates	250 MHz

Configuration Notes: R8051XC-EP– 2 timers/counters; 1 serial interface; 2-priority/5-source interrupt controller. Does not include full on-chip debug: OCDS implemented with two hardware breakpoints will add about 5,000 gates.

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Verification

The R80515XC-A core's functionality was verified by means of a proprietary hardware modeler. The same stimulus was applied to a hardware model that contained the original Intel 80C31 and Siemens SAB80C537 chips, and the results compared with the core's simulation outputs. The core was also verified through extensive functional simulation, and has achieved high code coverage results. The core satisfies the requirements of the Reuse Methodology Manual and VSIA Quality IP Metric.

Deliverables

The core is available in ASIC (synthesizable HDL) or FPGA (netlist) forms, and includes everything required for successful implementation:

- ASIC cores: HDL RTL source code
FPGA cores: Post-synthesis EDIF netlist
- An example implementation with sample system
- Sophisticated self-checking HDL Testbench including everything needed to test the core (Verilog versions use Verilog 2001)
- Simulation scripts, vectors, and expected results
- Synthesis or place and route script
- Comprehensive user documentation, including a detailed specification and a system integration guide