

# CAST

## R80251XC

Fast, Configurable,  
80251-Compatible  
Microcontroller Core

This 80251-compatible IP core implements a range of fast microcontrollers that execute the MCS® 251 instruction set and legacy code for the MCS® 51 instruction set.

The R80251XC IP core requires a single clock per machine cycle and runs an average of 3.18 times faster than the original 80C251 chip at the same clock frequency.

Dhrystone 2.1 test results of 0.098 to 0.23 DMIPS/MHz (depending on features) show the core runs up to 24.5 times faster than the original 80C51 and up to 2.22 times faster than the 80C251 at the same clock frequency.

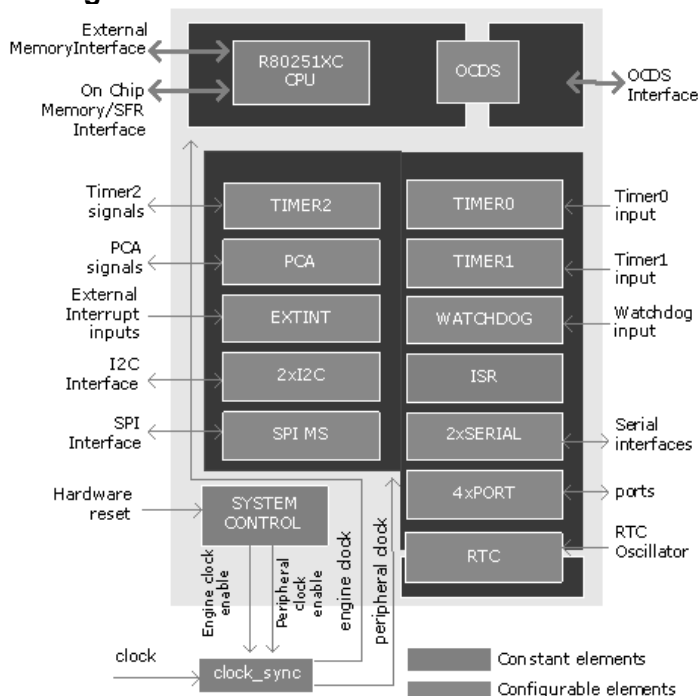
The core has a rich set of optional features and peripherals. Designers can choose from several versions, including the easy-to-configure full version with all options included and a variety of pre-packaged versions. System development is facilitated through the EASE native on-chip debugging option and support of Keil's C251 integrated development environment.

This new product builds on CAST's experience with hundreds of 8051 IP customers going back to 1997. Designed for easy reuse in ASICs, structured ASICs, or FPGAs,. Representative ASIC results show the core to be conservative in its use of space, requiring just 20,000 to 53,000 gates when optimized for area.

### Applications

Legacy code support with faster performance makes the core suitable for economically developing new systems by extending existing systems with new capabilities.

### Block Diagram



### Features

- Fully compatible with the MCS® 251 instruction set
- Single clock per cycle and efficient architecture for up to 3.18 times the performance of original 80C251
- Fewer machine cycles mean lower average power usage
- EASE Debugging option: On-Chip Debug Support (OCDS) block interfaces through IEEE1149.1 (JTAG) port; external debugging pod with JTAG and USB; debugging software with interface to Keil C251 tools

### Options and Peripherals

Full user-configurable version includes all of these; other versions include a subset (see Versions).

- External Memory Interface with 24-bit linear address space of up to 16 MB of Program and Data Memory
- On-chip RAM Interface that services up to 1kB of memory
- Special Function Registers Interface services from 43 to 115 external SFRs
- 40 bytes of Register File available as bytes, words or double words in a single clock cycle
- 8-byte instruction queue
- 64KB of extended stack space
- Two clock per cycle (legacy mode) supported
- Binary Mode (legacy 8051 compatibility) or Source Mode of operation (extended 80251 compatibility)
- Programmable wait-states for code and data memory
- Power Management Unit with power-down modes (IDLE/STOP)
- On-Chip Debug Support (OCDS)
- Parallel Ports: up to four 8-bit Input/Output ports
- Serial 0 interface: Full-duplex UART/USRT (80C51-like)
- Serial 1 interface: Full-duplex UART (80C517-like)
- Timers: up to three 16-bit timers (80C251-like)
- Programmable Counter Array
- Watchdog Timer: 14-bit programmable
- SPI Master/Slave interface
- One or Two I2C™ Master/Slave interfaces
- Real Time Clock

## Functional Description

The core is partitioned into modules as shown in the block diagram and described below.

### CPU (Central Processing Unit)

Fetches instructions from program memory, stores them in an 8-level queue, and executes using RAM or SFRs or Register Block as operands. Provides the ALU for 8- and 16-bit arithmetic, logic, multiplication and division operations, and Boolean manipulations. The RAM interface can address up to 1K bytes of Read/Write Data Memory Space, and up to 128 bytes of built-in and off-core Special Function Registers. The memory interface can address 16 MB of Program Memory and Data Memory. It eases the connection to memories using a de-multiplexed address/data bus, however a multiplexed interface is also available as part of the legacy 80C251 compatible mode. The variable-length code and data read/write to access fast or slow program memory is provided.

### Timers 0 and 1

Each has these three modes: 13-bit timer/counter, 16-bit timer/counter, and 16-bit timer/counter with auto reload. Timer 0 has an additional mode: two 8-bit timers. Each timer can also count external pulses (1 to 0 transition) on the corresponding t0 or t1 pin. Another option is to gate the timer/counter using an external control signal, which allows it to measure the pulse width of external signals.

### Timer 2

Operates as a timer, event counter, or bound rate generator, or a programmable clock-out generator.

In timer mode, it can be incremented every 12 clock cycles. In event counter mode, it is incremented when an external signal changes from 1 to 0 (sampled every machine cycle). Timer 2 is incremented in the cycle following the one in which that transition was detected. In gated timer mode, its incrementing is gated by an external signal.

The 16-bit timer/counter counts up or down depending on the settings. This module is also equipped with two 8-bit reload/capture registers.

### 4xPort

Controller serves up to four parallel 8-bit I/O ports to be used with off-core buffers. It is compatible with the classic 80C251, but the multiplexed memory bus feature can be excluded when selecting an enhanced CPU version. Alternate port functions are not implemented inside the core, allowing for flexible use of each peripheral separately. (These could be combined off-core if required).

### 2xSerial

Two fully independent serial ports for simultaneous communication over two channels. They can operate in identical or different modes and at different communication speeds. Serial Port 0 is capable of both synchronous and asynchronous transmission, while Serial 1 provides asynchronous mode only.

In synchronous mode, the microcontroller generates a clock and operates in half-duplex mode. In asynchronous mode it can operate in full-duplex mode. Received data is buffered in a holding register, which allows the serial ports to receive an incoming word before the software has read the previous value.

Serial Port 0 offers three communication protocols: Synchronous mode, with fixed baud rate; 8-bit UART mode, with variable baud rate; and 9-bit UART mode, with variable or fixed baud rate. Serial Port 1 has two operating modes: 8- and 9-bit UART mode, with variable baud rate. Both Serial Ports include an additional Baud Rate Generator.

### ISR (Interrupt Service Routine Unit)

The R80251XC provides an 80C251-compatible interrupt controller with four priority levels and up to twenty interrupt sources. Each source has its own request flag(s) located in a dedicated SFR.

### PCA

The Programmable Counter Array performs compare and capture functions. For the compare function, values stored in five 16-bit compare/capture registers are compared with the contents of a 16-bit timer. The results are signaled on the "cexo" outputs and interrupts are generated.

For the capture function, actual timer/counter contents can be saved into one of five 16-bit registers upon an external event or software request.

### 2xI2C (Primary and Secondary I2C™ Interfaces)

The primary (I2C) and secondary (SEC\_I2C) I2C Bus Controllers each provide a serial interface that meets the Philips I2C bus specification v1.0 and support all master/slave receiver/transmitter modes. Each is a true multi-master bus controller, including collision detection and arbitration to prevent data corruption if two or more masters simultaneously initiate data transfer. They perform 8-bit oriented, bi-directional data transfers up to 100 Kbit/s in the standard mode, or up to 400 Kbit/s in the fast mode.

### Serial Peripheral Interface (SPI) Interface

Provides full-duplex, synchronous communication between the core and other peripheral devices, including other MCUs. It can operate either as Master or Slave, with programmable clock rate, phase, and polarity. The maximum data rate is  $\frac{1}{4}$  of the system clock for a Slave, and  $\frac{1}{2}$  of the system clock for a Master. Write collision and overrun detection protect data, and Master mode fault detection for multi-master systems prevents bus conflict.

### Watchdog Timer

A 14-bit counter that is incremented every 12 system clock cycles. Once enabled it can only be cleared but remains counting until it reaches an overflow, thus generating a reset signal to the entire core. To avoid unintended use, a specific two-byte write sequence to the SFR register is required to enable or clear the watchdog timer.

## System Control

Generates clock enable signals for the main CPU and for peripherals; serves Power Down Modes IDLE and STOP; and generates an internal synchronous reset signal (upon external reset, watchdog timer overflow or software reset condition).

The IDLE mode leaves the clock of the internal peripherals running. Power consumption drops because the CPU is not active. Any interrupt or reset will wake the CPU.

The STOP mode turns off all internal clocks. The CPU will exit this state with an external interrupt or reset. Internally generated interrupts (timer, serial port, watchdog, etc.) are disabled since they require clock activity.

The Wake-up From Power-Down Mode allows two external interrupts to combinationally force the clock enable outputs back to active state so the clock generation can be resumed.

## RTC (Real Time Clock)

Provides a real-time count with a resolution of 1/256th second and range of 179 years. It can set and read seconds, minutes, hours, day of the week, and the date, represented by a 16-bit number interpreted by software. An alarm function can generate interrupts periodically or at a specific time, and these may be used to wake up from IDLE/STOP mode.

## OCDS

Internal block and JTAG port interface for the optional EASE debugging system. It provides the following functions: Run, Stop, Single-step; Software breakpoint; Debugger program execution; Hardware breakpoints; Read/Write Access to Program Memory, External/Internal Data Memory and SFRs; and Program Trace and Data Trace (optional).

## Implementation Results and Performance

The core's architecture eliminates redundant bus states and implements parallel processing of fetch, execution and write-back phases. Since a cycle is aligned with memory fetch when possible, most of the 1-byte instructions are performed in a single cycle.

The core uses one clock per cycle which leads to significant performance improvements with respect to the original Intel device operating with the same clock frequency.

Dhrystone 2.1 tests show the core having from 0.098 to 0.23 DMIPS/MHz depending on the features selected. This translates in an improvement of 24.5 times faster than the original 80C51, and up to 2.22 faster than the 80C251 at the same clock frequency.

## Available Versions

Six versions of the core are available, offering a range of capabilities and prices.

- **R80251XC** includes all options, and is user-configurable (options may be included or excluded prior to synthesis).
- **R80251XC-C** includes a custom set of options specified by the customer, and is not user-configurable.
- **R80251XC-I** includes options that match the original Intel 80C251 peripheral set: three timers, PCA, serial port, four parallel I/O Ports, two external interrupts, and a watchdog timer. These options are user-configurable (i.e., may be deleted prior to synthesis).
- **R80251XC-IF** version derived from the R80251XC-I, but is fixed and not user-configurable.
- **R80251XC-T** includes options that match the original Intel 80C251 with enhanced performance including: three timers, PCA, serial port, four parallel I/O Ports, two external interrupts, and a watchdog timer. These options are user-configurable (i.e., may be deleted prior to synthesis).
- **R80251XC-TF** version derived from the R80251XC-T, but is fixed and not user-configurable.

ASIC (RTL) and FPGA (netlist) deliverables are available; FPGA packages are not user-configurable.

The native EASE debugging package is an extra option for all versions.

## Implementation Results

R80251XC reference designs have been evaluated in a variety of technologies. The following are sample results using optimization for area.

ASIC Technology	Area		Speed (Min/Full)
	Min. Version	Full Version	
TSMC 65nm	33,775 $\mu\text{m}^2$ , 21,110 gates	77,841 $\mu\text{m}^2$ , 48,650 gates	29 MHz / 24 MHz
TSMC 90nm	57,681 $\mu\text{m}^2$ , 20,437 gates	148,801 $\mu\text{m}^2$ , 52,721 gates	25 MHz / 22 MHz

The following are sample results using optimization for speed for the full version.

ASIC Technology	Area	Speed
TSMC 65nm	179,999 $\mu\text{m}^2$ , 112,500 gates	226 MHz
TSMC 90nm	250,658 $\mu\text{m}^2$ , 88,810 gates	135 MHz

## Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available; contact CAST Sales.

## Verification

The core has been verified through extensive simulation and rigorous code coverage measurements.

All subcomponents were functionally verified with an HDL testbench using their individual test suites. The CPU and ALU have been verified against a proprietary hardware modeler and behavioral models. The peripherals have also been verified in their own testbenches, based on either hardware or behavioral models.

An extensive constrained random verification was performed to verify the CPU and OCDS

## Deliverables

The core is available in ASIC (synthesizable HDL) or FPGA (netlist) forms, and includes everything required for successful implementation. ASIC versions include:

- HDL RTL source code
- Behavioral model
- Easy-to-use configuration tool (with configurable versions)
- An example chip implementation, which uses the core in a sample system
- Sophisticated self-checking HDL Testbench including everything needed to test the core (Verilog versions use Verilog 2001)
- Simulation script, vectors, and expected results
- Synthesis script
- Comprehensive user documentation, including detailed specifications and a system integration guide

A reference design board is available; contact CAST Sales for information.

## Example Application

