The L8051XC1 megafunction implements an MCS®51-compatible microcontroller that is specially designed to match the timing and peripherals of legacy 8051 MCU based systems.

The megafunction can be configured to execute an instruction every 12, 6, or 4 clock cycles. Architectural extensions are user-selectable, including multiple data-pointers, a multiply-division unit, and a power management unit. Furthermore, the 8051 CPU can be coupled with a wide range of peripherals matching the behavior and timing of peripherals found in legacy architectures from Intel, Phillips/NXP, Siemens/Infineon, Maxim/Dallas, Texas instruments and others. Several pre-configured versions are offered; custom variations are also available.

The L8051XC1 runs legacy code, but new software development is facilitated through CAST’s on-chip debugging option, and debug pods that cooperate with Keil’s C51 integrated development environment.

This new product builds on CAST’s experience with hundreds of 8051 IP customers going back to 1997. Designed for easy reuse in ASICs, structured ASICs, or FPGAs, the megafunction is strictly synchronous, with positive-edge clocking (except in the optional debug & SPI modules), synchronous reset, and no internal tri-states. Representative Cyclone-IV results show the megafunction to be conservative in its use of FPGA resources, requiring just 2,000 to 11,500 LEs.

**Applications**

The L8051XC1 MCU megafunction is especially effective for extending the lifetime of existing systems where an originally-used discrete 8051 chip is difficult to replace, or the designer wishes to consolidate a multi-board system into a single FPGA or ASIC.

**Block Diagram**

![Block Diagram](image)
Available Versions

Three standard versions of the megafunction are available, offering a range of capabilities and prices.

- **L8051XC1-A** includes options that match the original Intel 8051 peripheral set: 64KB memory interface, two timers, one serial port, four parallel I/O Ports, two-level interrupt controller, and two DPTR registers. These options are user-configurable (i.e., may be deleted prior to synthesis).

- **L8051XC1-B** includes options that match the Infineon 80515/80517 peripheral set: 64KB memory interface, three timers, two serial ports, four parallel I/O ports, watchdog timer, multiplication-division unit, and two DPTR registers. These options are user-configurable (i.e., may be deleted prior to synthesis).

- **L8051XC1-C** custom/user-defined architectural and peripheral options. This version may integrate user-defined peripherals that are not supported by the automatic configuration tool. Please consult with your CAST sales contact to discuss your specific requirements and get lead time information.

ASIC (RTL) and FPGA (netlist) deliverables are available; FPGA packages are not user-configurable.

Implementation Results

L8051XC1 designs have been evaluated in a variety of technologies. The following are sample Altera results that are obtained after speed optimization during synthesis and place and route, while assuming that all megafunction I/Os are routed off-chip.

### Table 1: Sample Implementation results for CycloneIV-C6

<table>
<thead>
<tr>
<th>Configuration</th>
<th>Logic Utilization (LEs)</th>
<th>Fmax (MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>L8051XC1-CPU (CPU-only)</td>
<td>1,932</td>
<td>90</td>
</tr>
<tr>
<td>L8051XC1-A (Timer 0 &amp; 1, Serial 0, 4 parallel ports)</td>
<td>2,684</td>
<td>75</td>
</tr>
<tr>
<td>L8051XC1-CF (Timer 0, 1 &amp; 2, WDT, RTC, SPI, 2 I2C, Serial 0 &amp; 1, 4 parallel ports, MDU, DMA, 8 DPTRs, DPTR Arith, OCDS)</td>
<td>11,532</td>
<td>51</td>
</tr>
</tbody>
</table>

### Table 2: Sample Implementation results for CycloneV-C8

<table>
<thead>
<tr>
<th>Configuration</th>
<th>Logic Utilization (ALUTs)</th>
<th>Fmax (MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>L8051XC1-CPU (CPU-only)</td>
<td>1,287</td>
<td>76</td>
</tr>
<tr>
<td>L8051XC1-A (Timer 0 &amp; 1, Serial 0, 4 parallel ports)</td>
<td>1,814</td>
<td>68</td>
</tr>
<tr>
<td>L8051XC1-CF (Timer 0, 1 &amp; 2, WDT, RTC, SPI, 2 I2C, Serial 0 &amp; 1, 4 parallel ports, MDU, DMA, 8 DPTRs, DPTR Arith, OCDS)</td>
<td>8,498</td>
<td>43</td>
</tr>
</tbody>
</table>

The provided figures do not represent the higher speed or smaller area for the megafunction and area figures do not include any memories.

**Support**

The megafunction as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available; contact CAST Sales.

**Verification**

The megafunction has been verified through extensive simulation and rigorous code coverage measurements. All subcomponents were functionally verified with an HDL testbench using their individual test suites. The CPU and ALU have been verified against a proprietary hardware modeler and behavioral models. The peripherals have also been verified in their own testbenches, based on either hardware or behavioral models. An extensive constrained random verification was performed to verify the CPU, DMA and OCDS.

**Deliverables**

The megafunction is available in ASIC (synthesizable HDL) or FPGA (netlist) forms, and includes everything required for successful implementation. ASIC versions include:

- HDL RTL source code
- Easy-to-use configuration tool (with configurable versions)
- An example chip implementation, which uses the megafunction in a sample system
- Sophisticated self-checking HDL Testbench including everything needed to test the megafunction (Verilog versions use Verilog 2001)
- Simulation script, vectors, and expected results
- Synthesis script
- Comprehensive user documentation, including detailed specifications and a system integration guide

A reference design board is available; contact CAST Sales for information.