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CAST Releases USB OTG IP Core

February 2, 2004 (DesignCon) Santa Clara, California — Semiconductor intellectual property (IP) provider CAST, Inc. today announced the immediate availability of an IP core that implements the On-The-Go (OTG) supplement to the USB 2.0 specification.

USB OTG promises to build on the popularity of USB (Universal Serial Bus) by making it even easier to connect digital products. Whereas USB needs a computer host to manage the connection to one or more devices (a master-slave protocol), OTG gives every device enough host capabilities so they can be directly interconnected. Users will be able to, for example, connect their OTG-equipped camera directly to a printer for photos or to a cell phone for Internet sharing, without the use of a computer. (See www.everythingusb.com/usbonthego for more information.)

CAST's core conforms to the USB Implementer Forum's 2001 OTG supplement to the USB 2.0 high-speed specification. Ready for use in ASICs or FPGAs, the core implements a port that can serve as either a master or a slave when connected to another USB device. It offers an efficient design, with special hardware handling the host negotiation protocol (HNP), session request protocol (SRP), and other time-critical functions.

Designers can take advantage of the core's FIFO interfaces, and can program up to 16 IN and OUT endpoints to further optimize the core for their specific application. The CUSB2-OTG core includes a flexible, user-programmable general interface to 8/16/32-bit microprocessors. AMBA and other standard interfaces will be available soon.

A complete test environment helps designers verify the functioning and compliance of their OTG core. This environment includes a behavioral model of the PHY software layer to allow easy transaction simulation, as well as detailed specifications and full user documentation.

Sample implementations using single IN and OUT endpoints and optimization for speed show the core yields competitive area and performance results:

| Technology | Approx. Area | Maximum Frequency (interfaced processor clock) |
|--------------------------------|--------------|---|
| ASIC UMC 0.18 μ process | 21,000 gates | 186 Mhz |
| Altera Cyclone EP12C20-6 | 4,4843 LEs | 90 Mhz |
| Xilinx Virtex II Pro 2VP7-6 | 2398 SLICES | 71 MHz |

The CUSB2-OTG core was developed by CAST partner Evatronix SA, based in Poland (www.evatronix.pl). The core's pricing varies by configuration and license type; contact CAST for details.

About CAST, Inc.

CAST provides general purpose IP (gIP), offering nearly 100 different popular and standards-based cores including processors, interfaces, and application-specific functions for multimedia and encryption. ASIC, FPGA, and System-on-Chip (SoC) designers use these cores to significantly shorten their development time and reduce their overall costs. The company has about 200 customers developing products in nearly every applications area.

Privately owned and operating since 1993 with a focus on making IP practical and affordable, CAST has established a reputation for high-quality IP products, simple licensing, and responsive technical support. The company is headquartered near New York City, has a European office in the UK, and works with an international network of IP developers and distributors.

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