

CAST

ALTERA®

I2CS

Slave Bus Controller Megafunction

The I2CS Bus Controller logic provides a serial interface that meets the Philips I2C bus specification and supports all slave transfer modes to and from the I2C bus. The I2CS logic handles bytes transfer autonomously. It also keeps track of serial transfers, and a status register (i2cssta) reflects the status of I2CS Bus Controller and the I2C bus.

Developed for easy reuse with ASICs or FPGAs, the megafunction requires under 900 ASIC gates.

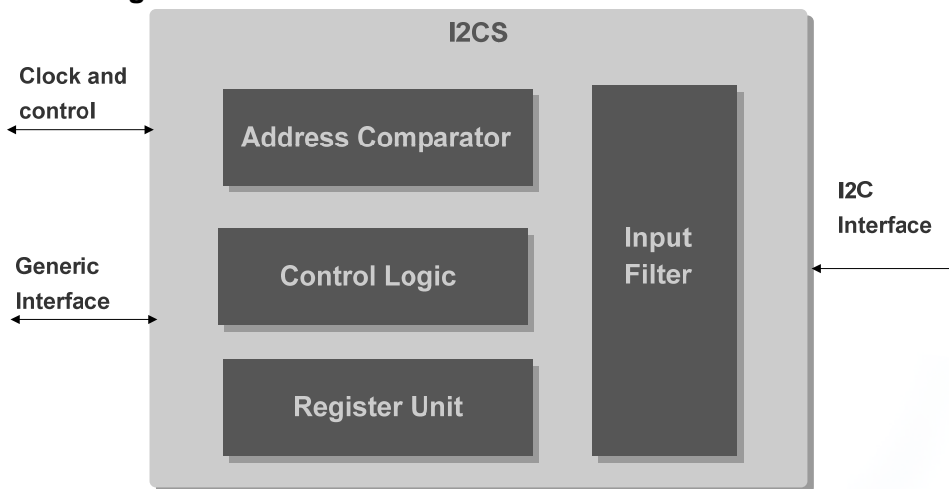
Applications

The I2CS can be utilized for a variety of serial interface applications.

Benefits

- I2C provides a convenient interface to I2C bus – the de facto world standard in a broad range of applications
- I2C uses only 2 wires to connect to virtually an unlimited number of devices, therefore minimizing interconnections and usage of IC pins in the user application
- I2C standard implements a simple and efficient bus which does not require additional logic such as address decoders or arbiters

Block Diagram



Features

- Uses two wires to transfer information between devices
 - Serial Clock Line SCL (SCL)
 - Serial Data Line (SDA).
- Performs serial transmission with data transfers up to 100 Kbps in standard mode and up to 400 Kbps in fast-mode
- Slave Receiver Mode - Serial data and the serial clock are received through SDA and SCL
- Slave Transmitter Mode - Serial data is transmitted via SDA while the serial clock is input through SCL
- Bi-directional data transfer
- Own address and General Call address detection
- 7 bit addressing format
- Fixed data width of 8 bits
- Data transfer in multiples of bytes
- One-byte write and read buffer
- Strictly synchronous design with positive-edge clocking, no internal tri-states and a synchronous reset; therefore scan insertion is straightforward

Functional description

The I2CS core is partitioned into modules as shown in figure above and described below.

Control logic

The control logic generates the control signals for serial byte handling.

Input filter

Input signals are synchronized with the internal clock (*clk*), and spikes shorter than three oscillator periods are filtered out.

Address comparator

The comparator compares the received 7-bit slave address with its own slave address. It also compares the first received 8-bit byte with the general call address (00H). If equality is found, the appropriate status bits are set and an interrupt is requested.

Register Unit

Address Register. The microprocessor can read from and write to this 8-bit, directly addressable SFR. *i2csaddr* is not affected by the I2CS hardware.

Data Register. *i2csdat* contains a byte of serial data to be transmitted or a byte which has just been received. The CPU can read from and write to this 8-bit, directly addressable SFR while it is not in the process of shifting a byte.

Control Register. The CPU can read from and write to this 8-bit, directly addressable SFR. One bit is affected by the I2CS hardware: the *si* bit is set when a serial interrupt is requested

Status Register. The *i2cssta* is read only special function register. The three least significant bits are always zero. The five most The Status Register significant bits contain the status code. There are 17 possible status codes (see tables 9 to 11). When each of these states is entered, a serial interrupt is requested. All *i2cssta* values correspond to defined I2CS states

Implementation Results

The I2CS is a technology independent design that can be implemented in a variety of process technologies. The following are sample Altera results.

Supported Family	Utilization		Performance
	LEs	Memory	Fmax
Acex EP1K10E-1	258	-	99 MHz
Cyclone EP1C3-6	248	-	224 MHz
Stratix EP1S10-5	228	-	225 MHz
Stratix-II EP2S5-3	199	-	294 MHz

Support

The megafunction as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Verification

The I2CS megafunction's functionality was verified by means of a proprietary hardware modeler. The same stimulus was applied to a hardware model that contained the original Philips 80C552 chip, and the results compared with the megafunction's simulation outputs.

Configurability

- Hardware configurability features:
 - Glitch register: configurable glitch removal length from both clock and data lines
- Runtime configuration features:
 - Own address
 - Toggle general call address accept

Deliverables

The megafunction is available in ASIC (synthesizable HDL) and FPGA (netlist) forms, and includes everything required for successful implementation. The Altera version includes:

- Post-synthesis EDIF netlist
- Testbench(self checking)
- Simulation script, vectors, expected results, and comparison utility
- Place and route script
- Comprehensive user documentation, including detailed specifications and a system integration guide

Related Products

I2C-HS – is an I2C Bus Controller which provides a serial interface that meets the Philips I2C bus specification v.2.1, compliant with PVCI (Peripheral Virtual Component Interface) or AMBA® AHB interfaces.

I2C – is an I2C Bus Controller which provides a serial interface that meets the Philips I2C bus specification and supports all transfer modes from and to the I2C bus. The core is available with either a generic or AMBA® AHB interface.