



H16750

UART with FIFOs and IrDA Megafunction

The H16750 is a standard UART providing 100% software compatibility with the popular Texas Instruments 16750 device. It performs serial-to-parallel conversion on data originating from modems or other serial devices, and performs parallel-to-serial conversion on data from a CPU to these devices.

The H16750 can be run in either 16450-compatible character mode or FIFO mode, where an internal FIFO relieves the CPU of excessive software overhead.

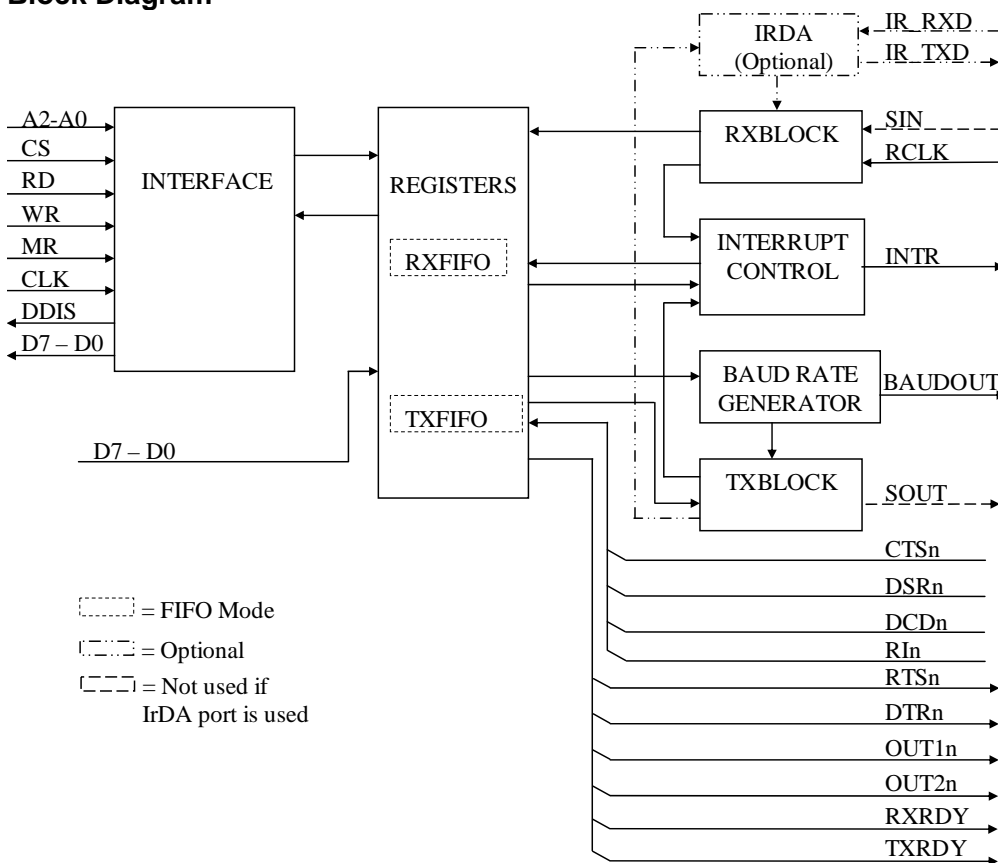
Developed for easy reuse in ASIC and FPGA applications, the H16750 is available optimized for several technologies with competitive utilization and performance characteristics.

Applications

The H16750 can be utilized for a variety of serial communication applications including:

- Serial or modem computer interface
- Serial interface within modems and other devices

Block Diagram



Features

- Capable of running all existing 16450 and 16550 software
- In FIFO mode, transmitter and receiver are each buffered with up to 256 byte FIFO's to reduce the number of interrupts presented to the CPU
- Available with FIFO sizes of 8, 16, 32, 64, 128 or 256 bytes
- Adds or strips standard asynchronous communication bits (start, stop and parity) to or from the serial data
- Independently controlled transmit, receive, line status and data set interrupts
- Programmable baud generator divides any input clock by 1 to $(2^{16} - 1)$ and generates the 16 x clock
- Independent receiver clock input
- Modem control functions (CTS_n, RTS_n, DSR_n, DTR_n, RIn, and DCD_n)
- Programmable Auto-CTS_n and Auto-RTS_n
- In Auto-CTS_n mode, CTS_n controls the transmitter
- In Auto-RTS_n mode, the receiver FIFO contents and threshold control RTS_n
- Serial Port has an optional Infrared Data Association (IrDA) data port
- Fully programmable serial interface characteristics:
 - 5, 6, 7, or 8 bit characters
 - Even, odd, or no-parity bit generation and detection
 - 1, 1½, or 2 stop bit generation
 - Baud generation
- False start bit detection
- Complete status register
- Internal diagnostic capabilities: loop-back controls for communications link fault isolation
- Full prioritized interrupt system controls

Functional Description

As shown in the Block Diagram and explained below, the H16750 includes seven major blocks: Interface, Registers, RXBlock, Interrupt Control, Baud Rate Generator, TXBlock and IrDA.

Interface

The Interface block is responsible for handling the communications with the processor (or parallel) side of the system. All writing and reading of internal registers is accomplished through this block.

Registers

The Registers block holds all of the device's internal registers. See the Register Description table for details on existing registers and their addresses. Some information comes from the other blocks, but this is all gathered together in the Registers block and made available to all blocks.

RXBlock

This is the receiver block. It handles the receiving of the incoming serial word. It is programmable to recognize data widths such as 5, 6, 7 or 8 bits, various parity settings such as even, odd or no parity and different stop bits of 1, 1½ and 2 bits. It checks for errors in the input data stream such as overrun errors, frame errors, parity errors and break errors. If the incoming word has no problems it is placed either in the Receiver Holding register or in the Receiver FIFO depending on the mode programmed.

Interrupt Control

The Interrupt Control block sends an interrupt signal back to the processor depending on the state of the FIFO and its received and transmitted data. There are various levels of interrupt which can be read from the Interrupt Identification register, which gives the level of interrupt. Interrupts are sent in the condition of empty transmission or receiving buffers (or FIFOs), an error in the receiving of a character, or other conditions requiring the attention of the processor.

Baud Rate Generator

This block takes the input clock, CLK, and divides it by a programmed value (from 1 to $2^{16} - 1$). This divided clock is then divided by 16 to create the transmission clock called the BAUDOUTn clock. This clock can be connected to the input clock (RCLK) to provide it with a proper clock.

TXBlock

The Transmit block handles the transmission of data written to the Transmission Holding register (or transmit FIFO). It adds required start, parity and stop bits to the data being transmitted so that the receiving device can do the proper error handling and receiving.

IrDA

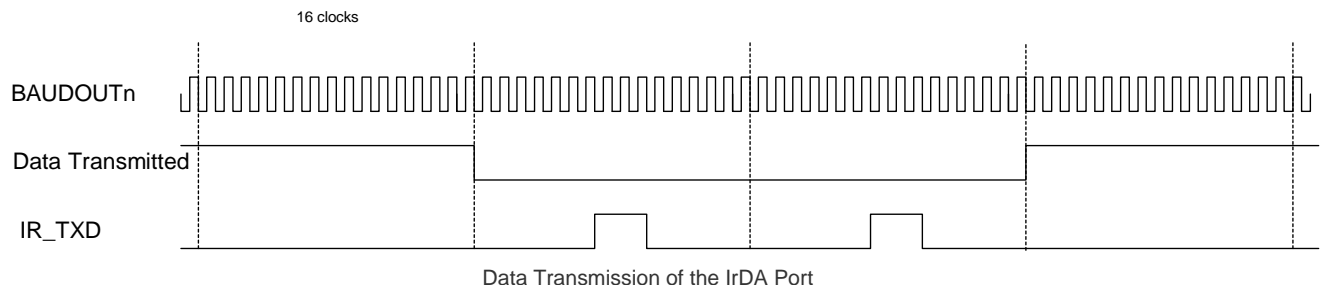
The IrDA block is an optional addition to the H16750. It handles the same data as the SIN and SOUT only in an Infra Red Interface format.

Optional IrDA Interface

The H16750 comes with an optional IrDA interface. This Infra Red interface works by replacing the wired SIN and SOUT pins. By connecting the Infra Red receiver and transmitter, the H16750 can be used in a “wireless” scenario.

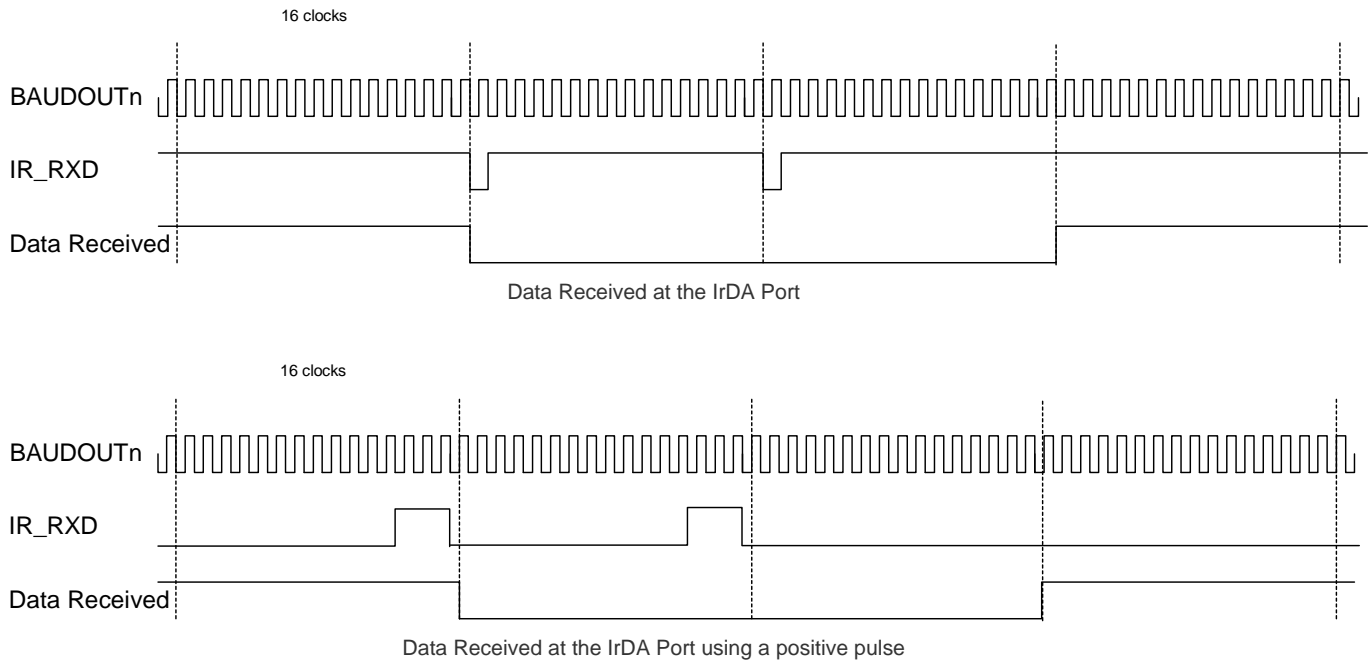
Transmitter

The format of the data is slightly different from the standard serial format that the H16750 uses. A bit for the H16750 is 16 BAUDOUTn clock cycles. The data output at the IR_TXD port is low at all times other than when transmitting a logic 0. For a logic 0, during the 7th through 10th BAUDOUTn clocks a logic 1 is transmitted (see the following diagram).



Receiver

Received data is a logic 1 unless the first clock of the 16 clock BAUDOUTn cycle has a falling edge. In that case, the received data is a logic 0. (see Figure 11). In Figure 12 the timing for a positive pulse input to the IrDA port is shown. Either one is usable without configuration.



FIFO Size Adjustment

The H16750 has an adjustable FIFO size. The size is changed permanently in the source code. Any netlist licenses have the FIFO size permanently set. Source code licenses have the opportunity to modify the FIFO size. This is done in the file *fifoctrl.vhd* in the src directory. The constant **CONFIG_FIFOSIZE** is set to the size desired and the constant **FIFO_ADDR_BITS** is set to the address size to match the FIFO. When FCR bit 5 is set (Alternate FIFO Enable) the Alternate FIFO Size is used. When not, a 16 Byte FIFO is used.

FIFO_ADDR_BITS	CONFIG_FIFOSIZE
4 (FCR – bit 5 = 1)	8
4 (FCR – bit 5 = 0)	16
5	32
6	64
7	128
8	256

Component Substitution

The H16750 megafunction is modeled after the Texas Instruments 16750. The following points differentiate the H16750 from the Texas Instruments device. In order to create a megafunction with the same functions a wrapper is required. A sample wrapper is included.

- No provision is made for a crystal. The CLK input is designed to accept a standard digital input.
- The bi-directional Data Bus has been split into an input and an output component. In order to use the megafunction with a bi-directional Data Bus the DDIS signal can be used as the controlling signal for the tri-state drivers.
- RDn, WRn, CS1 and CS2n have been eliminated. A single signal takes their place. These are RD, WR and CS.
- The ADSN signal has been removed. The H16750 functions as if the ADSN signal is held low. The included wrapper can be used to add the ADSN functionality latching the address and data buses.
- The main clock input CLK must be active from power-up.
- The Baudrate Generator is reset to the 0001h value upon activation of the MR signal. Programming the BRG to 0000h is an illegal value. The minimum value for the BRG is 0001h. Until the BRG is programmed, no output is generated.
- The Output Data Bus always shows the value of the last selected register.
- The Sleep and Low Power Modes are not modeled.
- The FIFO size is selectable to be either 8, 16, 32, 64, 128 or 256 bytes. This is done before synthesis.

- The trigger level is automatically adjusted to the FIFO size. It is programmable for 1 byte or 1/4, 1/2 or 7/8 of the maximum FIFO size.
- The H16750 comes with an optional IrDA interface.

Implementation Results

H16750 reference designs have been evaluated in a variety of technologies. The following are sample Altera results for a 64-byte FIFO implementation, optimized for speed, and assuming all megafunction I/Os are routed off-chip.

Version	Supported	Utilization			Fmax
	Family	LEs	Memory	Memory bits	(MHz)
No IrDA	Cyclone EP1C20-6	617	2 M4Ks	1216	116
	Stratix EP1S20-5	617	2 M4Ks	1216	126
	Stratix-II EP2S60-3	525	2 M4Ks	1216	175
With IrDA	Cyclone EP1C20-6	631	2 M4Ks	1216	114
	Stratix EP1S20-5	631	2 M4Ks	1216	123
	Stratix-II EP2S60-3	546	2 M4Ks	1216	180

Support

The megafunction as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Verification

The megafunction has been verified through extensive simulation and rigorous code coverage measurements.

Deliverables

The megafunction is available in ASIC (synthesizable HDL) and FPGA (netlist) forms, and includes everything required for successful implementation. The Altera version includes:

- Post-synthesis EDIF netlist
- Wrapper for pin compatible replacement
- Testbench (self checking)
- Simulation script, vectors, expected results, and comparison utility
- Place and route script
- Comprehensive user documentation, including detailed specifications and a system integration guide