

CAST

ALTERA

CUSB

Universal Serial Bus Device Controller Core

The CUSB is a USB Device Controller that provides USB full speed function interface that meets the 1.1 revision of the USB specification. The CUSB logic handles bytes transfer autonomously and bridges USB interface to a simple read/write parallel interface. The CUSB can be customized and optimized for a specific application. It contains a set of Special Function Registers that is similar to the Cypress EZ-USB FX chip.

The microcode-free design was developed for reuse in ASICs and FPGAs. The design is strictly synchronous with positive-edge clocking, no internal tri-states and a synchronous reset. Scan insertion is straightforward.

Applications

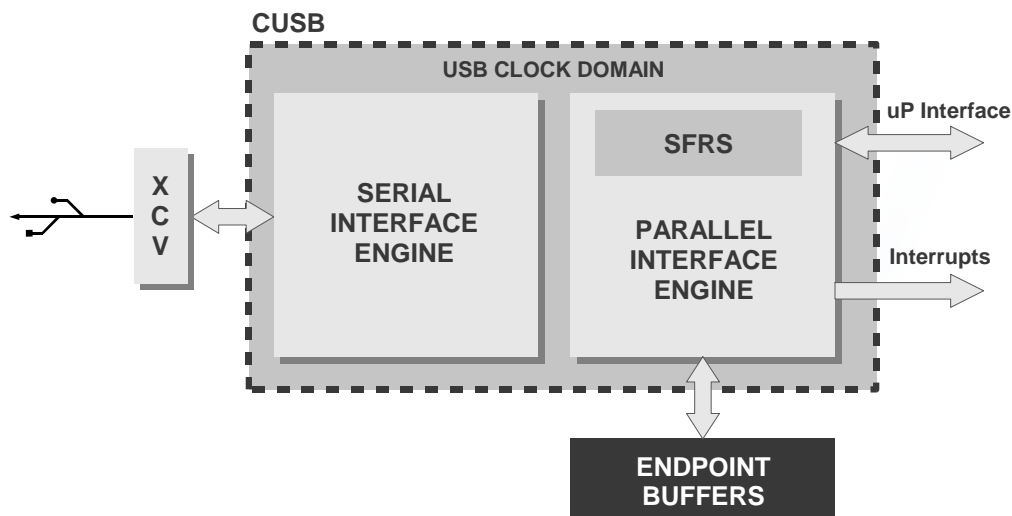
The CUSB can be utilized to provide a USB full speed function interface in a variety of applications including:

- Mass storage
- Audio
- Communication devices
- Digital cameras
- Digital media controllers

Software

A complete software stack configurable for the most popular device class is available. It has been designed for portability in a variety of embedded applications. It includes an intuitive Application Programming Interface (API) for application development.

Block Diagram



Features

- Serial Interface Engine
 - Support full speed devices
 - Extraction clock and data signals in internal DLL
 - NRZI decoding/encoding
 - Bit stuffing/stripping
 - CRC checking/generation
 - Interface for an external transceiver
- Up to 31 configurable endpoints
 - Support control transfers by endpoint 0
 - Support bulk, interrupt and isochronous transfers
 - Double buffering for isochronous endpoints
 - Programmable double buffering for bulk and interrupt endpoints
- Automatic data retry mechanism
- Data toggle synchronization mechanism
- Suspend and resume power management functions
- Remote Wake-Up function
- Endpoint buffers RAM interface
 - Up to 2 x 1024 Bytes FIFO size for isochronous endpoints
 - Up to 64 Bytes buffer size for each bulk, interrupt and control endpoints
- Microcontroller interface
 - Asynchronous address and data bus interfaces, and read and write control signals. (Internally synchronized within the CUSB core)
 - Interrupt request signals for application microcontroller
 - Interrupt vector for autovector interrupts

Optional Features

- DMA Controller
- Software stack
- On-Chip Peripheral Bus interface

Functional Description

The CUSB core is partitioned into modules as shown in the block diagram and described below:

Serial Interface Engine

As shown in the block diagram, the CUSB is connected directly to the USB transceiver. The CUSBSIE logic contains a Digital Phase Locked Loop (DPLL) that uses 4 times over-sampling USB data stream for clock extraction. It's able to track jitter and frequency drift as specified by the USB Specification Rev. 1.1. The CUSBSIE performs serial data decoding/encoding, bit stuffing/ stripping and CRC checking/generation. Received/ transmitted data are grouped in bytes and transferred to/from the CUSBPIE.

Parallel Interface Engine

The CUSBPIE contains a set of Special Function Registers (SFR) that are provided to control the CUSB behavior, the logic that handles all USB transfers and interfaces for endpoints buffers and for the microcontroller.

SFRS

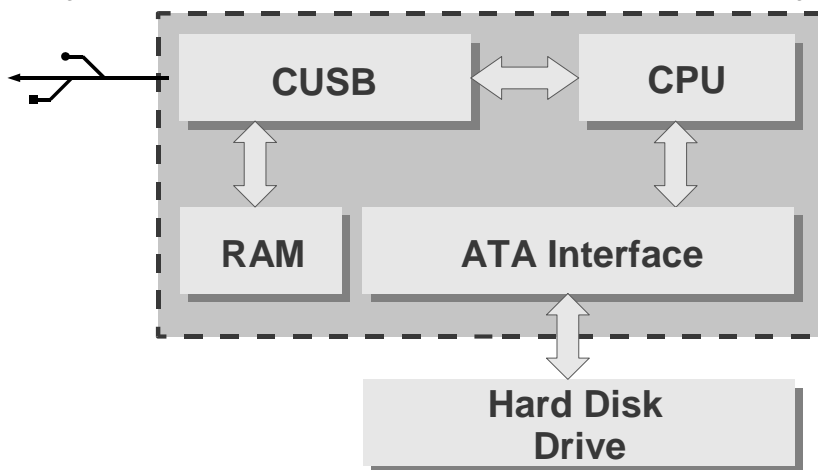
The SFRS contains set of Special Function Registers which are used to control the CUSB operation.

Support

The core as delivered is warranted against defects for three years from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Example Application

The diagram below demonstrates how the core can be used in a Mass Storage application.



The core is implemented with a dual port RAM, ATA Interface and CPU.

The Example application can work as USB peripheral. It transmits data between the HDD and PC using the USB connection. The CPU controls the settings of endpoints and services interrupts

Implementation Results

CUSB reference designs have been evaluated in a variety of technologies. The following are sample Altera results configured for operation with 1 BULK IN endpoint and 1 BULK OUT endpoint.

Supported Family	LE	Memory	IOB	Performance Fmax
Cyclone EP1C3-6	1165	6 M4Ks	49	48 MHz
Stratix EP1S10-5	1119	6 M4Ks	49	48 MHz
Stratix-II EP2S15-3	1046	6 M4Ks	49	48 MHz

Verification

The core has been verified through extensive simulation and rigorous code coverage measurements.

Deliverables

The core is available in ASIC (synthesizable HDL) and FPGA (netlist) forms, and includes everything required for successful implementation. The Altera version includes:

- Post-synthesis EDIF netlist
- Sophisticated HDL Testbench including external FIFOs, buffers, models of interfaces, and the core
- Simulation script, vectors, expected results, and comparison utility
- Place and route script
- Comprehensive user documentation, including detailed specifications and a system integration guide