



CPXP-EP

PCI Express Endpoint Controller Megafunction with SoC Bridge Extensions for AHB, AXI and Wishbone

Implements a PCI Express endpoint controller that is compliant with PCI Express Base specification 1.1, including the Transaction, Data Link, and Physical protocol layers. It is available to act as a bridge to standard buses including AMBA™ AHB, AMBA™ AXI and Wishbone.

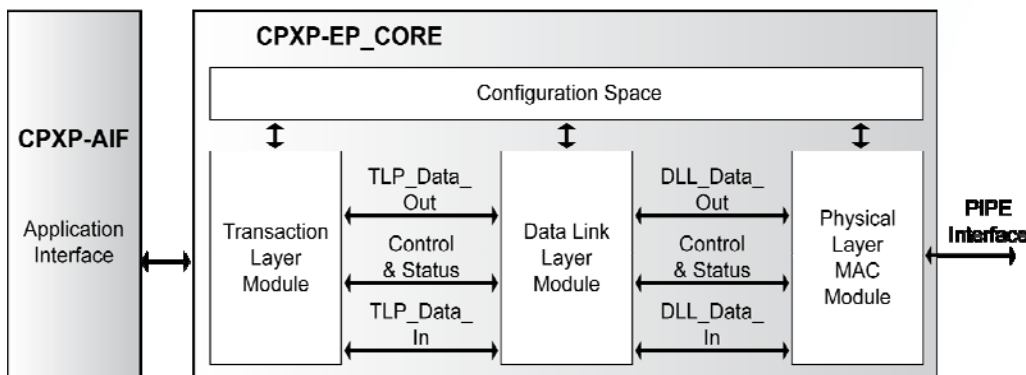
The scalable and flexible megafunction has a modular architecture and a high-performance, low-latency design. It supports multiple device link widths to better match the bandwidth needs of specific applications—x1 (single lane) and x4 (four lane)—and offers bi-directional data rates from 250MB/s (x1) to 1GB/s (x4). It supports most advanced PCI Express capabilities, including message signaled interrupts, multiple virtual channels, advanced error reporting, end-to-end cyclic redundancy check, and power management features. Multi-lane versions of the megafunction support lane reversal and polarity inversion.

The megafunction has an Application Interface (AIF) layer that makes integration significantly easier than the transaction layer packet (TLP) interface typically provided. This AIF includes a DMA controller and provides a higher-level connection between the megafunction logic and the user's application. Interfaces to standard system buses such as Wishbone or AMBA™ AHB are available.

The external connection interface from the megafunction conforms to the Intel® PIPE specification, ensuring compatibility with any 16-bit PIPE-compliant physical layer (PHY). The megafunction has been successfully used with PHYs from multiple vendors.

The synchronous, latch-free megafunction design was rigorously verified for compliance with the PCI Express specification, and has passed PCI-SIG certification. The megafunction has been tested for interoperability with multiple motherboards using chipsets from various vendors, and is in use by multiple customers.

Block Diagram



Features

- Compliant with PCI Express Base Specification 1.1
- Implements Transaction, Data Link, and Physical protocol layers in hardware
- Supports x1 and x4 link widths
- Offers a data rate of 2.5 Gbps per lane
- Supports up to eight Virtual Channels
- Supports lane reversal and polarity inversion
- PCI Configuration space type 0 header
- MSI capability support
- End-to-end cyclic redundancy code (ECRC) generation and checking support
- Advanced Error Reporting capability support
- Configurable TLP data payload size, from 128B to 4kB
- Configurable size for the Transmit Retry and Receive data buffers
- Modular architecture
- Synchronous design
- 64-bit internal datapath at 125MHz

Integration

- Application Interface (AIF) for easier system integration using industry standard bus interfaces (e.g., Wishbone, AMBA™); handles up to 8 DMA channels
- Conforms to standard PIPE interface for compatibility with any 16-bit PIPE-compliant PHY

Applications

PCI Express is rapidly being adopted for a variety of interconnection applications, including:

- Network server
- Graphics and multimedia
- Communications and mobile products
- Industrial, automotive, and other embedded system

Certification



The x1 and x4 versions of this megafunction have passed the PCI-SIG PCI Express compliance tests, and appear on their Integrators List.

Functional Description

The megafunction is divided into four modules responsible for the Configuration Space, Transaction Layer, Data Link Layer, and Physical Layer MAC.

Configuration Space

Provides a Configuration space register file type 0. In addition to the mandatory functions, numerous extended capabilities are also supported.

Transaction Layer Module

Responsible for the assembly and disassembly of transaction layer packets. The transaction layer supports four address spaces: Configuration space, Memory space, I/O space and Message Space. Power management services are supported.

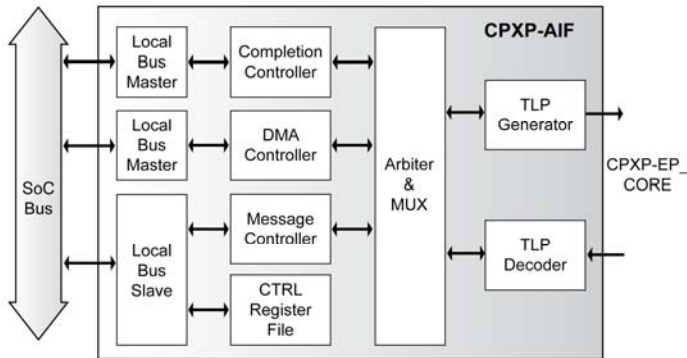
Data Link Layer Module

Responsible for link management, data protection and integrity checking, retry and power management services.

Physical Layer MAC Module

Implements the logical sub-block of the physical layer. The module is responsible for link training and status monitoring, link width negotiation, lane order negotiation, lane polarity reversal control and power management implementation.

SoC Bus Bridge (Application Interface Module)



The SoC Bus bridging feature is added via an additional module called AIF which adds direct SoC bus connectivity with up to 8 DMA channels fully programmable from both the PCIe and SoC busses. The AIF provides a higher-level interface that makes system integration easier than working at the TLP level. The AIF bridge is available for standard SoC buses including AMBA™ AXI, AHB and Wishbone.

The Completion Controller automatically handles read and write requests, and sends completions if needed.

The configurable DMA Controller provides up to eight independent DMA channels.

Implementation Results

CPXP-EP reference designs are being evaluated in a variety of technologies; the results from 1 and 4 link widths implementations of the megafunction are shown below (at the required frequency of 125 MHz, with a single VC, no ECRC, max. payload 256B, 2kB Retry buffer and 4kB Receive buffer).

Supported Family	Link Width	ALUTs	IOBs	Memory (bits)	GXB	PLL	Tool Version
Stratix II GX 2SGX90-3	x1	8,371	7	49,408	1	1	6.0 SP1
Stratix II GX 2SGX90-3	x4	10,816	19	49,408	4	1	6.0 SP1
Arria GX 1AGX60-6	x1	7,545	7	49,408	1	1	7.1 SP1
Arria GX 1AGX60-6	x4	10,401	19	49,408	4	1	7.1 SP1

Note: Only PCI Express bus interface signals are routed off-chip

The megafunction includes an Application Interface (AIF) extension, an additional subsystem for integrating the megafunction with SoC designs using custom or various standard interfaces.

Support

The megafunction as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Verification

The megafunction has passed PCI-SIG certification and has been verified using Avery's PCI-Xactor verification tool. Interoperability has been verified with Intel, nVidia, VIA, and SIS chipsets, and PHYs from GeneSys Logic, Altera, and others have been successfully used by CAST and customers.

Deliverables

The megafunction is available in ASIC (synthesizable) or FPGA (netlist) forms, and includes everything required for successful implementation. The Altera version includes

- Post-synthesis netlist of the CPXP-EP and CPXP-EP-AIF
- Sophisticated HDL Testbench including external FIFOs, buffers, models of interfaces, and the megafunction
- Simulation script, vectors, expected results, and comparison utility
- Place and route script
- Comprehensive user documentation