



ATAIF

ATA-7/IDE Host Controller Megafunction

Implements a host controller for non-volatile memory devices using the parallel interface known as ATA (Advanced Technology Attachment), IDE (Integrated Drive Electronics), and ATAPI (Advanced Technology Attachment Packet Interface). Complies with standard ATA-7.

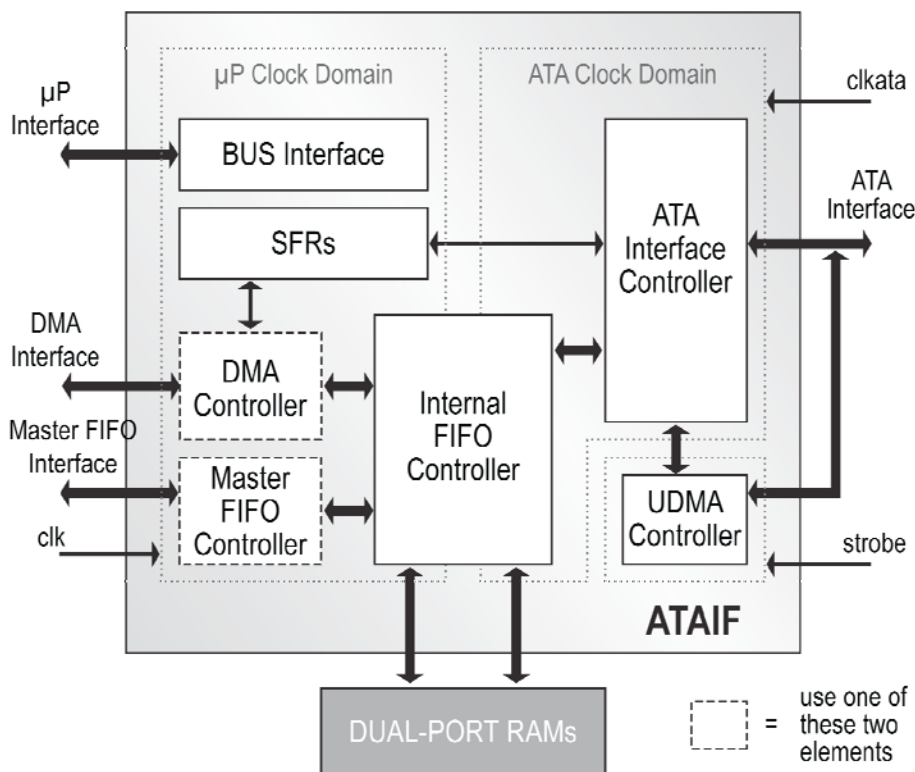
The megafunction provides a simple interface to memory devices such as hard-disk drives, DVD players, CDROM players/writers, Compact Flash storage, and PC Card devices. It supports PIO modes 0 to 4; Multi-word DMA modes 0, 1 and 2; Ultra ATA - 33, -66, -100 and -133; and implements an interface to the IDE bus.

Developed for easy reuse in ASIC and FPGA implementations, the megafunction is strictly synchronous, with positive-edge clocking, no internal tri-states, and a synchronous reset; scan insertion is straightforward.

Applications

- IDE disk drive, CDROM player/writer & DVD player controllers
- Compact Flash and PC-Card readers
- Systems utilizing IDE/ATA and ATAPI drives for data storage including notebook and desktop computers, servers, set-top boxes and test equipment
- Data acquisition systems

Block Diagram



Features

- Complies with ATA-7 Standard
- Supports one or two IDE devices
- Supports synchronous Ultra ATA-33, -66, -100 and -133
- Configurable parameters allow easy tailoring of megafunction to specific application or implementation technology
- Programmable I/O modes: 0, 1, 2 and 4
- Multi-word DMA modes: 0, 1 and 2
- Generic SFR interface with configurable data bus: 8/16/32-bit
- Configurable Internal FIFO address bus width: min. 4-bit, no upper limit
- Configurable transmission counter size: from 2- to 32-bit
- Use either the DMA Controller or the Master FIFO Controller for the data transmission interface
- DMA Controller provides synchronous data transmission interface
 - Master and slave mode
 - Configurable data bus: 8/16/32-bit
 - Configurable address bus: min. 8-bit, no upper limit
- Master FIFO Controller data transmission interface
 - Configurable data bus width: 16- or 32-bit
 - Easy direct connecting to CUSB2, CUSB2-OTG or USBHS-OTG-SD CAST megafunctions
- Transmit/Receive buffers operate as internal configurable FIFOs
 - Configurable FIFO depth
 - Configurable 16/32 bit data bus (when the Master FIFO Controller interface is used)
- Sophisticated self-checking Testbench (Verilog versions use Verilog 2001)

Functional Description

The megafunction is partitioned into modules as shown in the block diagram and described below.

ATA Interface Controller

Contains the PIO, MDMA and UDMA state machines. These control the ATA Interface working in PIO modes 0 to 4; Multi-word DMA modes 0, 1 and 2; and Ultra ATA -33, -66, -100 and -133 modes.

Also parallel data CRC generation for UDMA transfers.

UDMA controller

Contains buffers for input data, used while the megafunction executes Ultra DMA transfers.

DMA Controller (optional)

Used for data transmissions, working as a master or a slave system data bus (according to settings in the SFRs). Can be replaced by the Master FIFO Interface Controller.

Master FIFO interface Controller (optional)

Controls the Master FIFO interface, which can be used to integrate the ATA Interface Controller with USB controllers (e.g., CAST megafunctions CUSB2, CUSB2-OTG or USBHS-OTG-SD). Can be replaced by the DMA Controller.

Internal FIFO Controller

Has two buffers used for buffering transmit and receive data inside the megafunction. Generates read/write signals for two on-chip Dual-Port RAMs.

SFRs

Contains a set of Special Function Registers used for controlling the megafunction.

BUS Interface

Controls the microprocessor bus interface. It provides a synchronous read/write interface to the SFRs that can be easily integrated with various processor systems.

Implementation Results

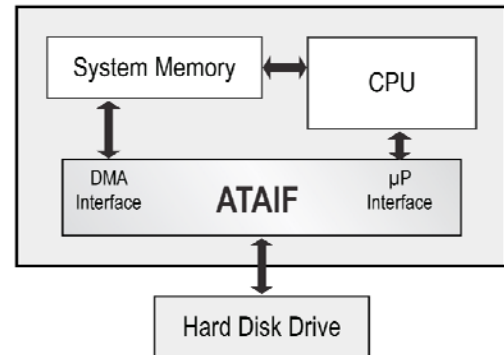
The megafunction has been evaluated in a variety of technologies. The following are sample Altera results with area optimized for speed, implemented with internal DMA controller, max. data bus sizes, and internal FIFO depth: 512 words.

Altera Technology	Area	ATA Clock	Processor Bus Clock Frequency
Cyclone EP1C4 6	3430 LCs + 8 M4Ks	100 MHz	135 MHz
Stratix EP1S10 5	3900 LCs + 8 M4Ks	133 MHz	140 MHz
Stratix II EP2S15 3	3280 ALUT + 8 M4Ks	133 MHz	205 MHz
Cyclone II EP2C20 6	3630 LCs + 8 M4Ks	133 MHz	145 MHz

See the web site for ASIC and more FPGA implementation results.

Example Application

Here the megafunction is used to send data from system memory to a hard disk drive. It uses the DMA Interface, and the CPU processes interrupts and controls the settings.



Support

The megafunction as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Verification

The megafunction has been verified through extensive simulation and rigorous code coverage measurements.

Deliverables

The megafunction is available in ASIC (synthesizable HDL) and FPGA (netlist) forms, and includes everything required for successful implementation. The Altera version includes:

- Post-synthesis EDIF netlist
- Sophisticated self-checking Testbench (Verilog versions use Verilog 2001) including an example system design and bus/behavioral model of interface stimulators
- Simulation script, vectors and expected results
- Place and route script
- Comprehensive user documentation, including detailed specifications and a system integration guide