CPU Subsystem Total Power Consumption

Understanding the Factors and Selecting the Best IP

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Overview

- Comparing Processor Power Ratings
- Understanding the Energy Impact of:
  - Processor Performance
  - Processor Area
  - Processor Code Size
  - Processor support to Dynamic Power Management

Please type in any Questions and we'll answer them after the presentation
(or email questions to me later)

The µW/MHz Quest

Process Node	Synthesized Frequency	Power Consumption	Silicon Area
28HP	100 MHz	2.3 µW/MHz	0.01 mm²
40LP	100 MHz	4.4 µW/MHz	0.01 mm²
65LP	100 MHz	8.6 µW/MHz	0.03 mm²
90LP	100 MHz	10.3 µW/MHz	0.05 mm²
180LP	100 MHz	69.2 µW/MHz	0.22 mm²

* All results are for template processor configuration. Frequency is slow process corner, nominal Vdd minus 10%, 125°C, SVt only. Power consumption is typical process, nominal Vdd, 25°C. Area is floorplanned, excluding RAMs. Additional details available upon request.

low-power

very low-power

the lowest-power

Leakage current **	< 6.6 µW	-	6.6 µW
Dynamic Power consumption **	65 µW/MHz	-	95 µW/MHz

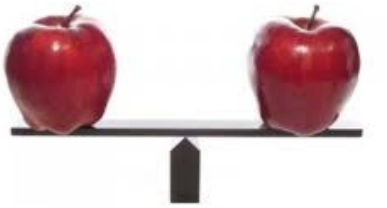
(*) In slow case conditions for TSMC 0.18 um GP process (1.62 V, 125°C)
(**) In typical case conditions for TSMC 0.18 um GP process (1.8 V, 25°C)
(1) Configuration 050:Core only
(2) Configuration 051:2 timers 16-bit, 1 UART, 1 interrupt controller, 1 GPIO module, 1 JTAG emulation interface, 1 breakpoint module

Vital Statistics

- 0.042 mm² in 90 nm
- 10.85 µW/MHz in 90 nm
- 400 MHz in 90 nm

- µW/MHz is like MPG but worse!
  - No standard driving cycle
  - No "City" and "Highway"
- Challenging to get comparable stats from different vendors
  - What process, library, or corner operating conditions?
  - What optimization, toggle activity, or tool flow?

Comparing Apples to Apples

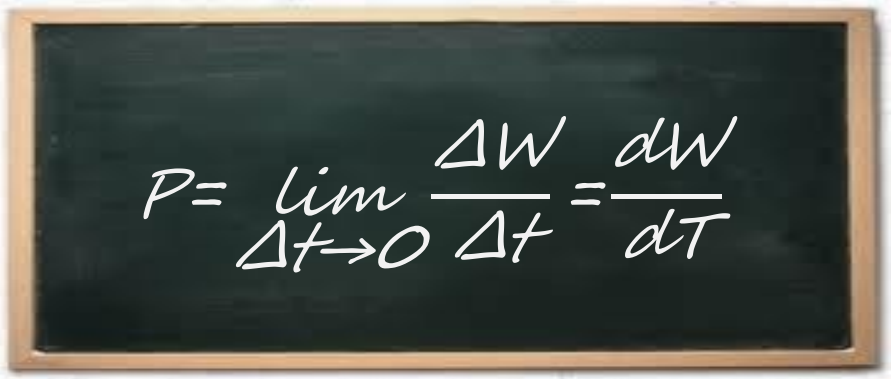


- "General-Purpose" vs. "Low-Power" at same geometry can be ≥50% greater
- Optimizing for speed and high frequency can use ≥50% more power than optimizing for area, power, and low frequency
- Activity statistics (i.e., software running on the processor) make a big difference in power estimates
- Look at the footnote for processor configuration, missing clock-trees, register files, etc.

Compare µW/MHz for your design!!!

µW/MHz Ratings Aren't Enough

- **Energy** is what gets consumed



- A processor's Energy Efficiency depends on:
  - Processor **Performance**
  - Processor **Area**
  - Processor **Code Size**
  - Ability to apply **Power Management**

Performance and Energy

- Higher performance allows doing more in less time, and sleeping for a longer time
  - Requires less energy to complete a given task
- Higher performance allows lower clock rates
  - Reduces clock tree and CPU power when active
  - Enables use of HVT cells and allows smaller implementation, both decreasing power leakage

Faster Processors can be more Energy Efficient!

- **Example 1**: Application requires the processor to deliver 100 DMIPS in 1 second and then sleep.

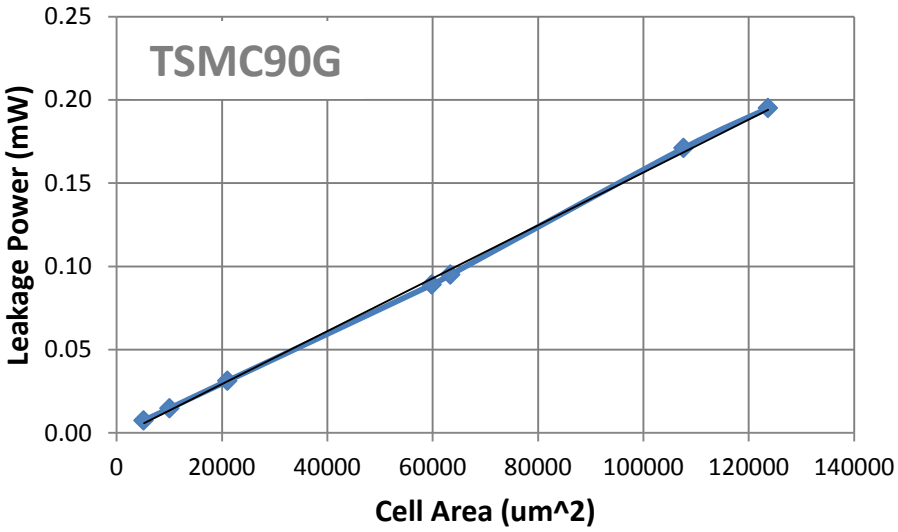
Processor	µW/MHz	DMIPS/MHz	Required Clock Freq. (MHz)	Time (Sec) to Complete the Task	**Energy (µJ) to Complete the task**
BA22	0.020	1.7	58.82	1.00	**1.18**
Cortex-M0	0.016	0.98	102.04	1.00	**1.63**
Cortex-M3	0.032	1.25	80.00	1.00	**2.56**

- **Example 2**: Processor runs at 50MHz and needs to deliver 200 DMIPS ASAP and then sleep.

Processor	µW/MHz	DMIPS/MHz	Clock Freq. (MHz)	**Time (Sec) to Complete the Task**	**Energy (µJ) to Complete the task**
BA22	0.020	1.7	50	**2.35**	**2.35**
Cortex-M0	0.016	0.98	50	**4.08**	**3.27**
Cortex-M3	0.032	1.25	50	**3.20**	**5.12**

Area and Energy

- With short active periods and long idle periods, idle energy can be equally or more important than active energy
- Leakage currents and therefore idle energy is more or less proportional to area



Smaller Processors can be more Energy Efficient!

- **Example 3:** Application requires the processor running at 10MHz to deliver 100 DMIPS every day

Processor	Active Power (µW/MHz)	Static Power (µW)	DMIPS/ MHz	Time to Complete the Task (sec)	**Energy to Complete the task (µJ)**	Idle Time per Day (sec)	Idle Energy per Day (µJ)	**Total Energy per Day (µJ)**
BA22 no MULDIV	0.015	0.0006	0.9	11.11	**0.17**	86388.9	51.8	**52.00**
BA22 with MULDIV	0.020	0.0010	1.7	5.88	**0.12**	86394.1	86.4	**86.51**

CPU or CPU + Memory?

	Active Power	Idle Power
Typical 32bit CPU @100 MHz, 90nm	5mW	0.01 mW
32KBytes SRAM Accessed@50MHz, 90nm	9mW	0.02-0.06 mW
OTP Read @ 10MHz, 90nm	5-50mW	~0
256Mb LP-DDR	180mW	3.5 mW (Standby) 0.01mW (idle)

Don’t lose sight of the forest for the trees!!!

Code Size and Energy

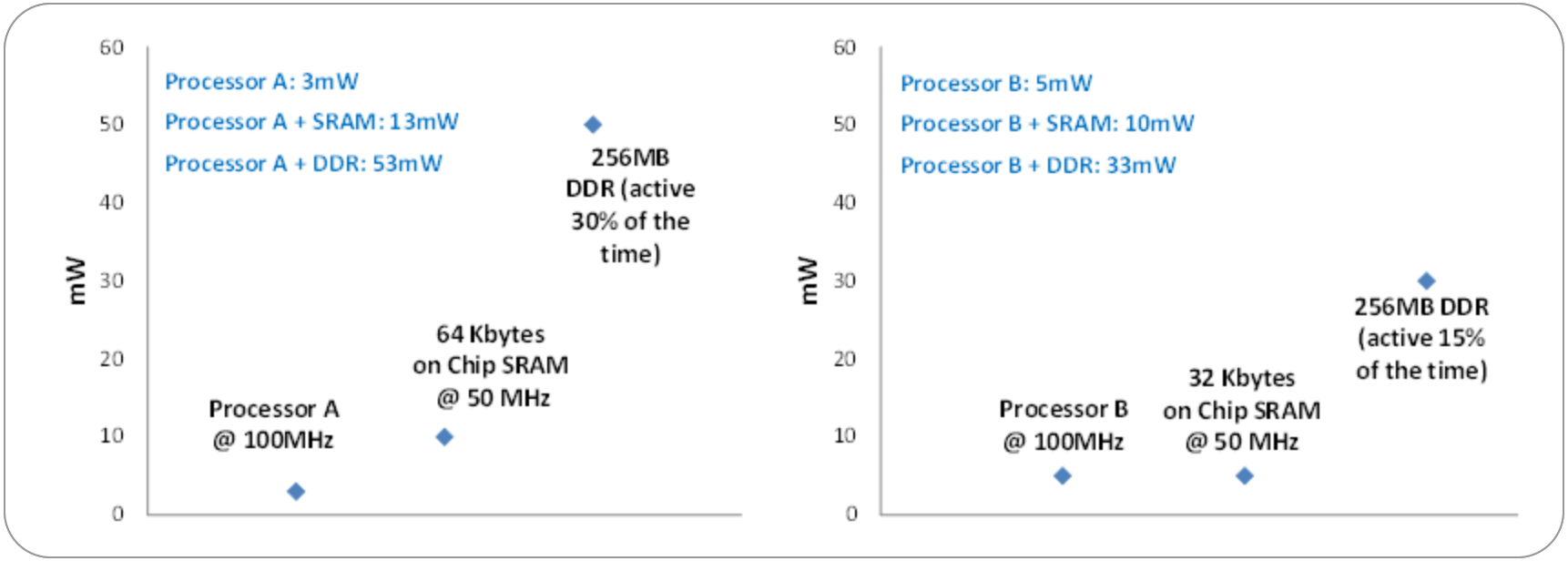
Smaller code means:

- Smaller instruction memory size
  - Lower energy cost per access
- Fewer instruction memory accesses for a specific task
  - Lower energy for a specific task
- Reduced I-cache misses
  - Fewer accesses to the power-hungry central memory

Code-Size-Efficient means Energy-Efficient!

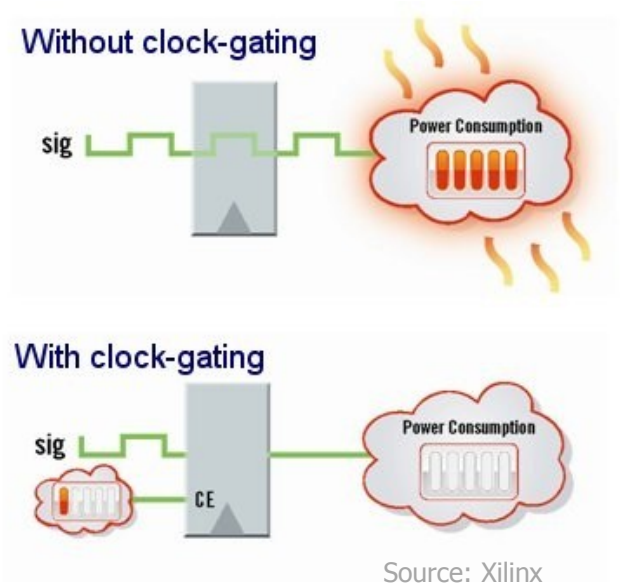
Example 4:

"Low-Power" Processor-A vs. "Code-Efficient" Processor B



Spare some µW/MHz for DPM?

- Dynamic Power Management (DPM) techniques can significantly reduce energy consumption
- With a few more µW/MHz, a processor can:
  - Automatically gates clocks to unused modules
  - Broadcast idle/active state and provide means to externally gate their clocks
  - Allow SW control over CPU and bus frequencies



Source: Xilinx

Putting it all together

The Easy Way

- Compare µW/MHz ratings

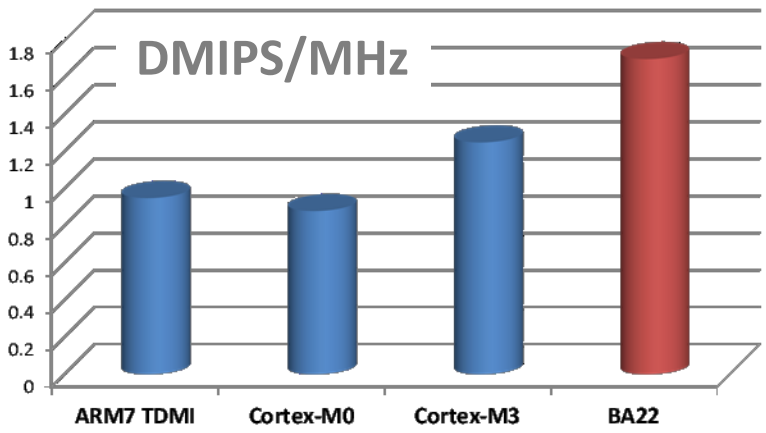
Work with your vendors to characterize the processor cores for your application

The Right Way

- Profile your application needs, and weigh active vs. idle power
- Assess energy impact of processing power & area
- Take into account code size and memory energy
- Make sure there are no roadblocks to DPM

BA22: Energy Efficient 360º

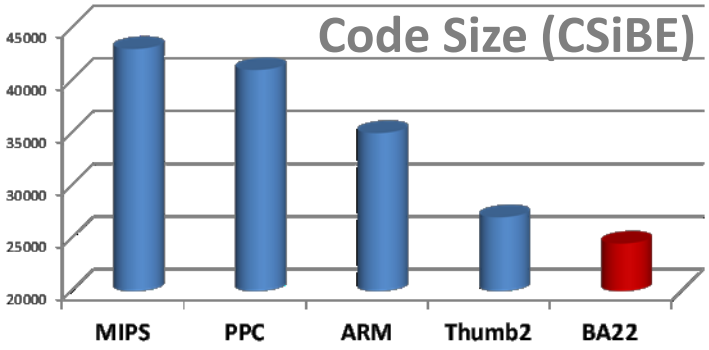
Powerful



Small and Low Power

0.02 µW/MHz (TSMC65LP)

15k-35k Gates (TSMC65LP)



Automatic Clock Gating

Separate Clocks and Status Broadcasting

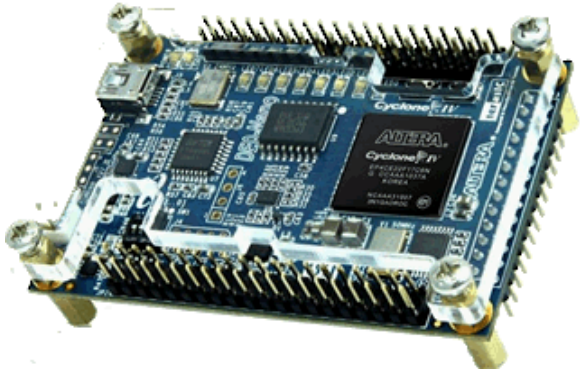
SW-Controlled Frequency Scaling

Advanced DPM Features

Extreme Code Density

Next Steps with CAST

- Learn more at http://www.cast-inc.com/ba22
- See for yourself:
  Try an evaluation to test
  the BA22 in your environment
  with your code



- Contact your local rep, or CAST Sales
  - Reps: http://www.cast-inc.com/sales/offices.html
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Thank you for your attention!

- Questions and Answers
- Post-Webinar Survey

Slides available on our website