

PCI Express Core Integration with the OCP Bus

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The logo for CAST, Inc. features the word "CAST" in a bold, red, sans-serif font. The letters are slightly shadowed, giving them a three-dimensional appearance as if they are floating above the background.

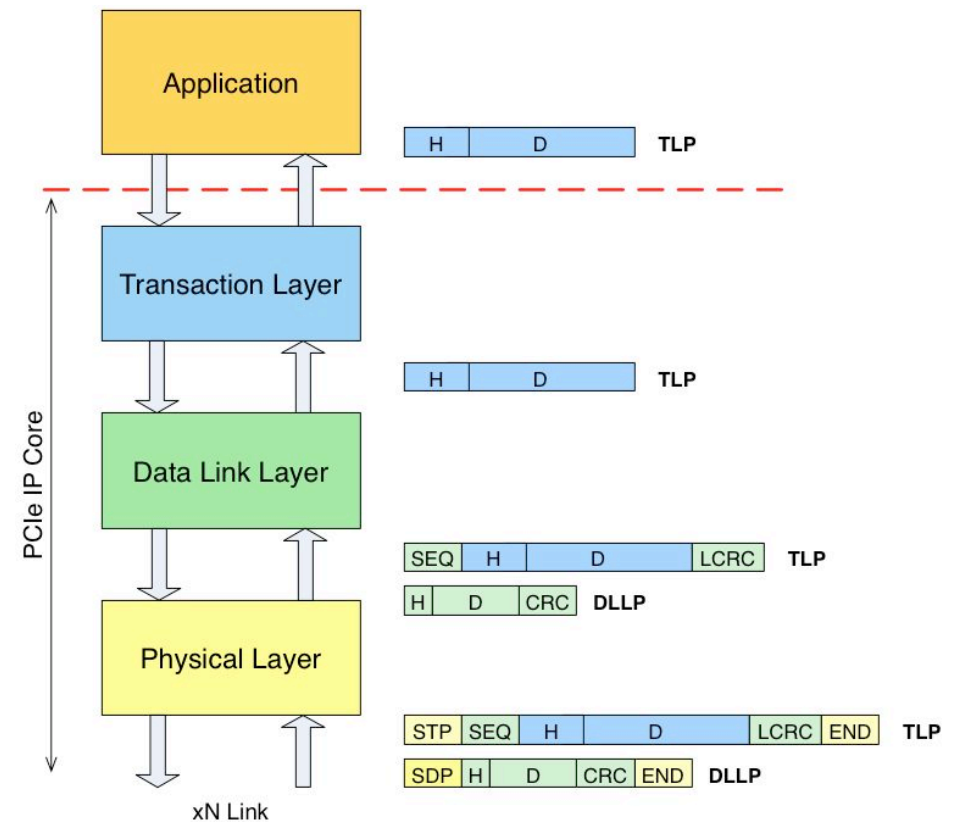
IP that Works
Experience that Counts

Overview

- ▶ PCIe core integration challenges
 - Understanding of spec
 - Transaction Layer Packet Details
- ▶ Possible approaches
 - Through examples
 - Through a proprietary interface
 - Through an Application Interface and standard bus
- ▶ Implementing an AIF for OCP
 - Hiding PCIe and OCP details
 - Delivering a complete solution

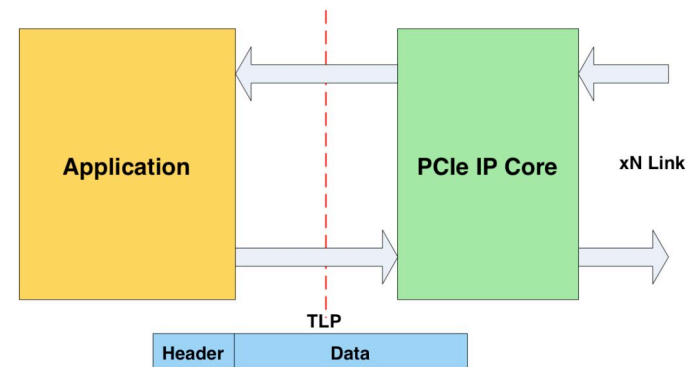
PCIe Design Layers

- ▶ PCIe is a high-speed serial bus
- ▶ Layered architecture
- ▶ Application Data transferred via packets
- ▶ PCIe IP cores usually implement the lower three layers
- ▶ PCIe IP cores solve most of the protocol handling
 - connection establishing
 - link control
 - flow control
 - power management
 - error detection and reporting



PCIe Core Design

- ▶ Endpoint Controller core handles internal PCIe details
- ▶ But typical core stops at the Transaction Layer Packet (TLP) interface
- ▶ Designer still required to understand PCIe details for TLP
 - correct packet decoding
 - correct packet forming
- ▶ Can impact many elements in application system

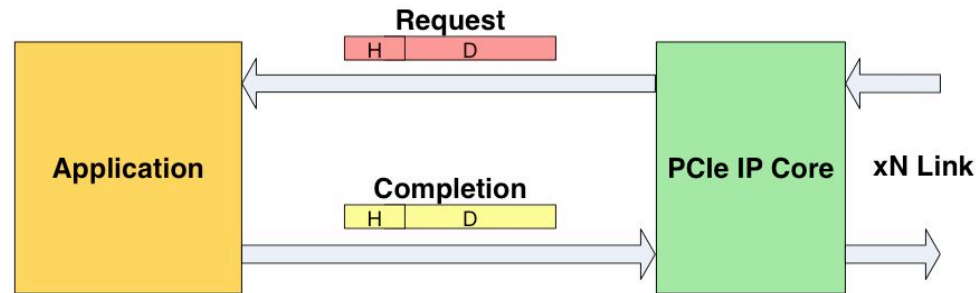


7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
R	Fmt X 0	Type						R	TC 0 0 0	Reserved						T D	P E	Attr 0 0 0	R	Length											
Requester ID								Tag								Last DW BE (0000)				1st DW BE											
Address [31:2]																R															

7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
R	Fmt X 1	Type						R	TC	Reserved						T D	P E	Attr	R	Length											
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Address [63:32]																															
Address [31:2]																R															

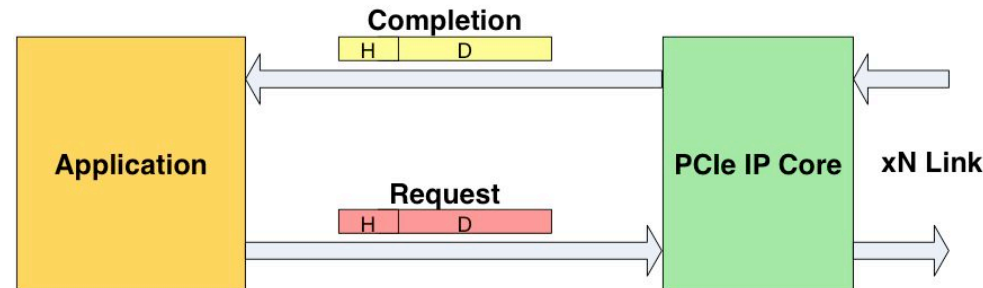
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
R	Fmt X 0	Type						R	TC	Reserved						T D	P E	Attr	R	Length											
Completer ID								Compl. Status				B C M				Byte Count															
Requester ID								Tag								R	Lower Address														

Incoming Requests



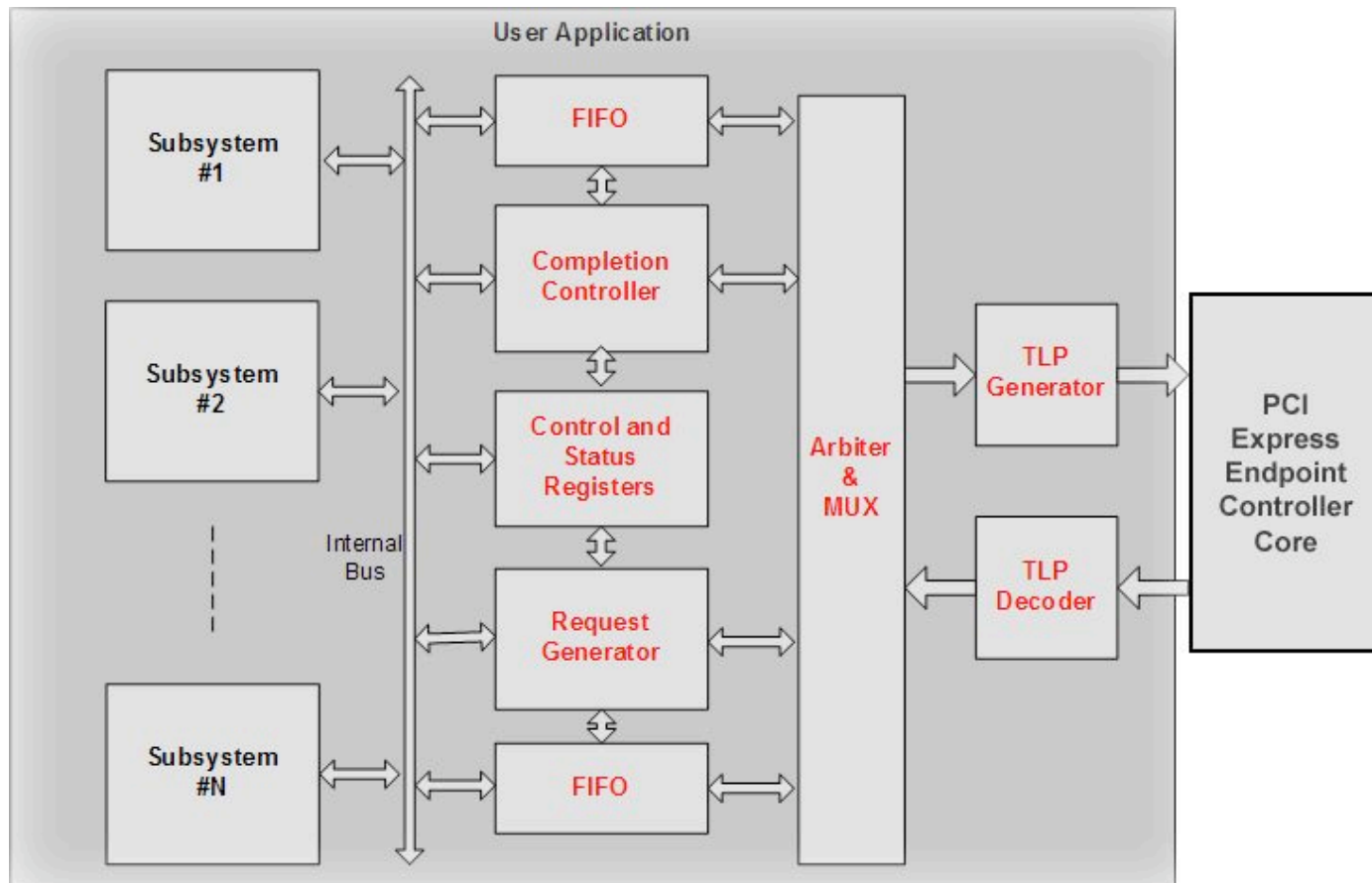
- ▶ Incoming requests perform local subsystem read or write
- ▶ Some incoming requests require sending completion TLP
- ▶ Completion TLP rules
 - Must form completion packets with respect to `Max_Payload` and `Read Completion Boundary`
 - Must correctly encode fields in completion TLP
 - Completion address in packet differs (I/O x Memory)
- ▶ Application must correctly report a request processing problem to the core

Outgoing Requests



- ▶ Outgoing Requests are generated by the application
- ▶ There is a set of rules for forming outgoing request TLP
 - Must be identified by unique Tag
 - Read requests restricted by `Max_Read_Request_Size`
 - Write requests restricted by `Max_Payload`
 - Must not cross 4kB address boundary
- ▶ Violations will result in request being discarded and error detected at receiver
- ▶ Completion request processing
 - Completions for multiple outstanding requests must be processed by Tag
 - Must have correct values in lower addresses to process multiple TLPs
 - Must process both `Unsupported Request` and `Completer Abort` responses

User Application Architecture



Possible Approaches

- ▶ PCIe IP core providers are aware of the design challenges
- ▶ Guiding by Design Examples
- ▶ Application interface module with a proprietary backend interface
- ▶ Application interface with a standard SoC bus interface

Guiding by Examples

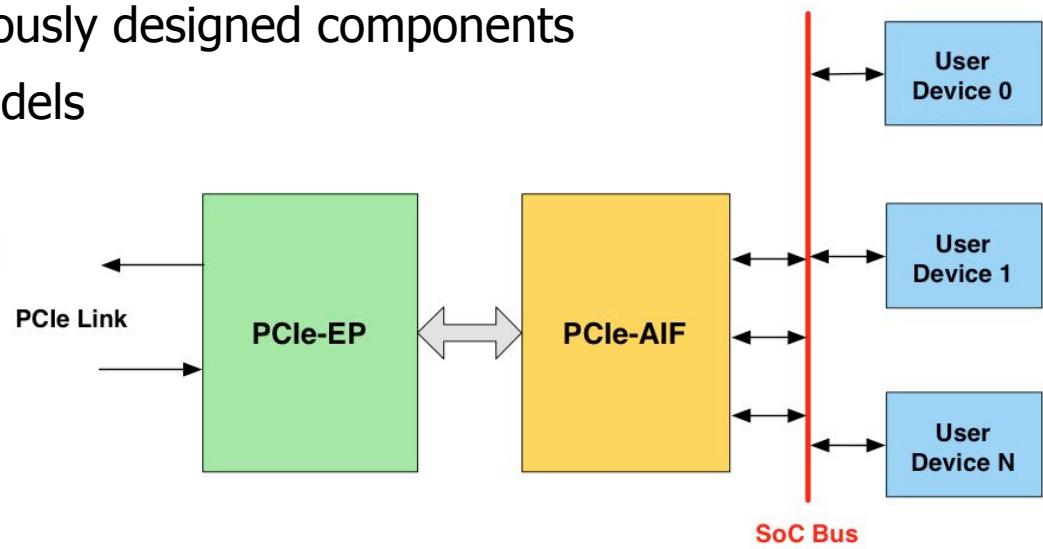
- ▶ Requirements
 - Deliverables should follow QIP Metric for quality & completeness, with extensive design examples illustrating TLP
- ▶ Designer duties
 - Understand PCIe specification
 - Implement interface and functional logic for incoming request processing
 - Implement a module for outgoing request generation and processing
 - Handle verification including PCIe compliance testing
- ▶ This approach
 - Can result in highly optimized small design
 - Requires more time for design and verification

Proprietary Application Interface

- ▶ Features
 - Custom completion controller for processing incoming requests
 - DMA channels to generate and process outgoing requests
 - Proprietary backend interface
 - Verification of PCIe protocol guaranteed by IP provider
- ▶ Designer Duties
 - Designer must learn new backend interface
 - Adopt application subsystems to interface with the proprietary interface
- ▶ This approach
 - Isolates designer from PCIe complexities
 - Subsystems not reusable in any other design unless modified

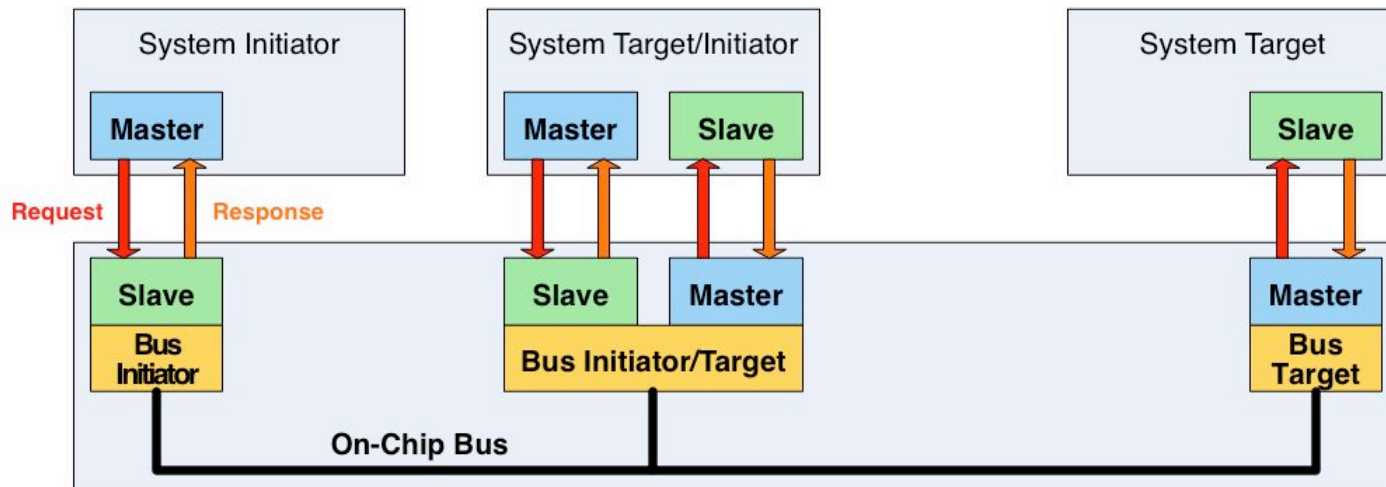
Application Interface with SoC Bus

- ▶ Similar to previous approach, but with industry-standard bus backend
- ▶ Using SoC bus interface offers significant advantages:
 - Already familiar to designer
 - Simple system architecture
 - Simple reuse of a previously designed components
 - SoC bus verification models available
 - The bridge fully verified by IP core provider



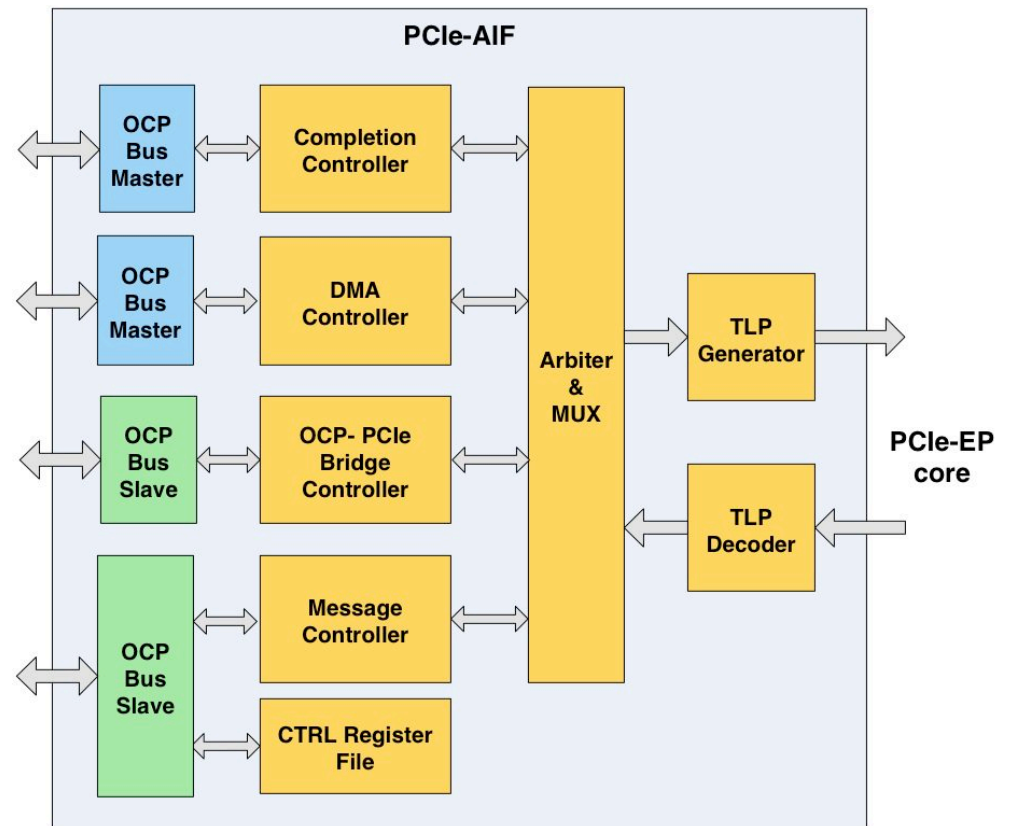
OCP Bus

- ▶ Well-defined SoC bus
- ▶ Point-to-Point connections with unique On-Chip Bus architecture
- ▶ Flexible extensions to the basic signal set
- ▶ SystemC models available for free



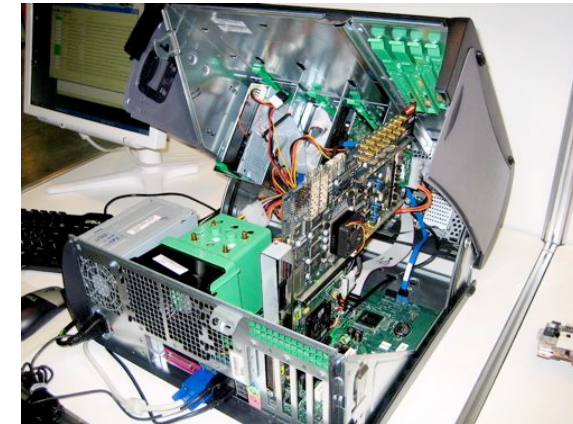
Implementing the AIF for OCP

- ▶ AIF bridges TLP interface and OCP bus
- ▶ Completion Controller with queued request processing
- ▶ DMA core with up to eight channels
- ▶ OCP-PCIe Bridge Controller
- ▶ Optional Message Controller

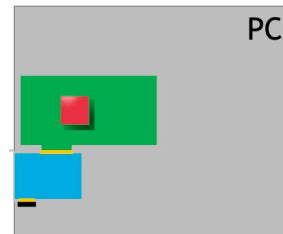


Verification & Reference Design

- ▶ Rigorously verified with Denali
 - PureSpec PCIe models
 - PureSuite compliance testsuite
- ▶ Implemented in reference design (Wishbone version)
- ▶ About to undergo PCI-SIG certification testing
- ▶ Live demo in DATE booth

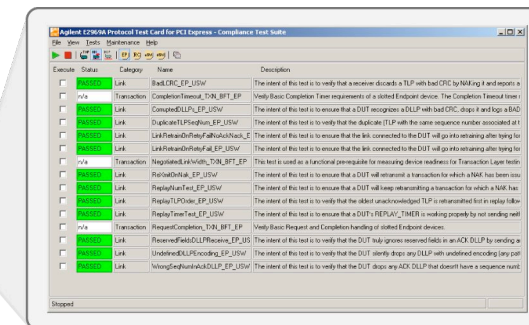


Virtex-II Pro
PCIe-EP
Core



E2969A
Agilent
Technologies
PCI Express
Protocol
Test Card

DN600K10SE
Dini Group
Prototyping
Board



Compliance Testing
Positive results satisfy PCI-SIG
certification requirements

Conclusions

- ▶ Integration challenges:
designer must understand PCIe to deal with TLP interface
- ▶ Of possible approaches, Application Interface (AIF) to standard bus is best
- ▶ AIF with OCP offers several advantages
- ▶ Implementation and certification underway