SoC Solutions Builds FPGA System in Record Time Using Synopsys' ReadyIP Flow and CAST IP Cores

Woodcliff Lake, NJ, June 4, 2008 — Silicon Intellectual Property (IP) provider CAST, Inc. and technical partner SoC Solutions LLC recently proved the effectiveness of a new FPGA design capability from Synopsys' Synplicity Business Group by developing a complete 32-bit processor-based system in just three and a half days.

The system is a typical design that uses an ARM® Cortex™-M1 processor and includes all the buses and peripherals needed to run embedded software. SoC Solutions' engineers estimate it took them less than half the time if would normally have taken them to create the system, which they demonstrated recently at the Embedded Systems Conference (ESC).

The quicker development was made possible by Synopsys' new ReadyIP initiative for technology-independent FPGA design. This includes the ReadyIP line of pre-packaged, pre-licensed evaluation cores—supplied by CAST and others—and the new System Designer capability included in the Synplify Pro® and Synplify® Premier FPGA implementation tools, that makes it easy to define and synthesize FPGA systems.

"Our experience with ARM processor-based systems and the IP infrastructure needed to make them work certainly helped, but the real advantage behind our fastest system development ever came from Synopsys' new ReadyIP program," said Jim Bruister, president of SoC Solutions.

 "FPGA designers for the first time have an independent system integration tool flow with easy access to popular third-party IP like that from ARM and CAST, that works across all FPGA vendors," said Bruister. "Companies now have a real opportunity to evaluate their designs using different FPGA vendors, and to easily migrate their entire systems between FPGAs and ASICs."

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Using the ReadyIP Program

Synopsys' ReadyIP program offers the first practical ability to easily acquire and integrate evaluation IP from multiple independent providers and target it to devices from multiple FPGA vendors.

Suppliers using the ReadyIP flow ensure consistent packaging and interconnection compatibility across the ReadyIP program by using the SPIRIT Consortium's IP-Xact metadata format. Their valuable IP is protected using the encryption technology with digital rights management (developed by the Synplicity Business Group of Synopsys and now undergoing standardization in the IEEE's P1735 Working Group). Vendors offer their cores through ReadyIP under simple, click-to-agree evaluation licenses, eliminating the red tape typically surrounding IP use and making possible the "push-button downloads" philosophy behind the ReadyIP program.

FPGA designers use a new IP browser built in to Synopsys' Synplify Pro and Synplify Premier tools to select and download ReadyIP partner cores, then use the System Designer tool to connect and configure the ReadyIP cores along with their own internal IP. Designers synthesize the resulting system to a target FPGA, and then evaluate their design and their FPGA decisions. Only when satisfied and ready for production do they need to purchase commercial licenses from the ReadyIP Program's core suppliers.

"The success that SoC Solutions achieved by using the new ReadyIP flow and System Designer capability is a testament to the fact that our standards-based tools simplify IP access and use," said Angela Sutton, product marketing manager, Synopsys Synplicity Business Group. "This technology, which is included in our Synplify Pro and Synplify Premier tools, provides embedded systems designers with an extremely productive path to implementing complex systems in FPGAs."

Implemented on a Synopsys HAPS-51 high-speed prototyping system, the ESC demo system ran a live software debugging session complete with two-way communication with a laptop PC through a Hyperterm window. The demo exercised the ARM Cortex-M1 processor and a comprehensive set of AMBA buses and peripherals, including the AHB and APB buses, an AHB to APB Bridge, Memory Controllers, Timer, UART, GPIO, PWM, and external FLASH and SRAM memories.

The system infrastructure library used in the demo system — called the PiP-AMBA — was developed by SoC Solutions and is part of the CAST product line. ReadyIP charter member CAST provided the greatest number of downloadable cores at the launch of the program, with samples from CAST's broad line of IP including a JPEG encoder and decoder, PCI Express controllers, an SDRAM memory controller, and other interface and communications functions.

More information is available on the web:

• CAST ReadyIP Cores — http://www.cast-inc.com/synplicity/

• SoC Solutions LLC — http://www.socsolutions.com/

• Synopsys ReadyIP Program — http://www.synplicity.com/partners/readyip/

• The SPIRIT Consortium and the IP-XACT standard — http://www.spiritconsortium.org/

• The OpenIP Encryption Standard — http://www.eda.org/ip-encrypt/

About Soc Solutions

SoC Solutions provides solutions for microprocessor based FPGAs, ASICs, ASSP, and Structured ASICs. SoC Solutions was founded in 2000 by experienced ASIC and Embedded Software designers with a rich history of designing ASICs with embedded microprocessors. Our Pre-integrated IP Platforms have been used successfully in numerous ASICs, FPGA and Structured ASIC designs. SoC Solutions is located in the Atlanta Georgia area.

About CAST, Inc.

CAST provides over 100 popular and standards-based IP cores for ASICs and FPGAs. Privately owned and operating since 1993, CAST has established a reputation for high-quality IP products, simple licensing, and responsive technical support. The company is headquartered near New York City, partners with IP developers around the world, and works with select sales consultants and distributors throughout Europe and Asia.

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