

## CAST PCI Express Core Achieves PCI-SIG Certification

**Woodcliff Lake, NJ, February 28, 2007** — Semiconductor intellectual property (IP) provider CAST, Inc. today announced that its PCI Express Endpoint Controller core has passed the rigorous interoperability and compliance testing of the PCI-SIG, and appears on the PCI Express Integrators List (at [www.pcisig.com](http://www.pcisig.com)).

CAST's CPXP-EP endpoint controller core is targeted at systems needing fast but lean data transfer and designers wishing to learn as little as possible about the inner workings of PCI Express. The core is ready for implementation in FPGAs or ASICs, works with standard external physical layer (PHY) chips, and offers a unique Application Interface layer for easy system integration.

The CPXP-EP core implements the transaction, data link, and physical protocol layers in compliance with the 1.0a PCI Express Base Specification, and provides an efficient x1 single-lane device link for bidirectional data transfer rates up to 250 MB/s. Extra features for error checking, configuration flexibility, and power saving are all included.

The core's external interface conforms to the Intel PIPE specification, ensuring compatibility with any 16-bit PIPE-compliant physical layer (PHY). The PCI-SIG testing was done in partnership with Genesys Logic, Inc., using their GL9714 PCI Express 8- or 16-bit PIPE-compliant PHY. The GL9714 is efficient and full-featured, has been silicon-proven at multiple technology nodes, and is used by hundreds of customers around the world. It passed PCI-SIG compliance testing in early 2006, and is listed on the PCI-SIG Integrators List. See [www.genesyslogic.com](http://www.genesyslogic.com) for more details on the GL9714 PCI Express PHY.

The controller core's internal interface features an Application Interface (AIF) layer that goes beyond the Transaction Layer Packet (TLP) interface of competing cores to greatly simplify the integration of PCI Express with a user's system. This AIF includes a DMA controller and other functions to automatically handle the complexities of interfacing with standard internal buses like Wishbone or AMBA AHB. This makes it easier to add PCI Express to these systems without the technical challenges of a TLP interface.

The core was rigorously verified using a commercial PCIe test suite and other means, and passed PCI-SIG testing its first time through. In addition to the Genesys Logic PHY, the core has been successfully implemented in FPGAs using the native Altera and Xilinx PHYs. It has also been tested for interoperability with motherboards using Intel, nVidia, VIA, and SIS chipsets, and is in use by multiple customers.

The CPXP-EP IP core was developed and is supported by CAST's engineering teams in the Czech Republic and New York City area. It is available now in RTL source code for ASICs or optimized netlists for structured ASICs and FPGAs. See the website for more information: [www.cast-inc.com](http://www.cast-inc.com).

## About Genesys Logic, Inc.

Founded in 1997, Genesys Logic is a fabless IC design house renowned for its leadership in high-speed I/O technologies. In 2003, it became the first company in the world to demonstrate working silicon of a fully PIPE-compliant PCI Express PHY. The company's U.S. office is located at 2860 Zanker Road, Suite 102, San Jose, CA 95134, USA and can be contacted at 1-408-435-8899 or [sales@GenesysAmerica.com](mailto:sales@GenesysAmerica.com). For more information about Genesys Logic Inc, visit <http://www.genesyslogic.com>.

## About CAST, Inc.

CAST provides over 100 popular and standards-based IP cores for ASICs and FPGAs. Privately owned and operating since 1993, CAST has established a reputation for high-quality IP products, simple licensing, and responsive technical support. The company is headquartered near New York City, partners with IP developers around the world, and works with select sales consultants and distributors throughout Europe and Asia.

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