

CAST adds 1-Gigabit Ethernet MAC and USB 2.0 IP Cores

March 4, 2003 (DATE'03) Munich, Germany — Semiconductor intellectual property (IP) provider CAST, Inc. today announced two new cores implementing popular networking and bus standards: the 1-Gigabit Ethernet Media Access Controller (MAC-1G), and the Universal Serial Bus version 2.0 Function Controller (CUSB2).

The new cores provide complete support of industry standards and make it quick and cost-effective for designers to incorporate high-speed Ethernet or USB in their systems. Designed for reliable reuse and packaged with verification aids and documentation, the cores are available in source form for ASIC synthesis or as netlists optimized for various programmable devices. They join the broad range of CAST general purpose IP (gIP) cores, which includes processors, other network and bus interfaces, multimedia and encryption functions, serial communications, and other popular functions. The CUSB2 core will ship in April; the MAC-1G in May.

About the 1-Gigabit Ethernet MAC Core

The CAST MAC-1G core is a flexible, full-featured implementation of the IEEE 802.3-2000 MAC specification. It includes a comprehensive host interface — with integrated FIFO logic and DMA controller — and can work with various data path widths and system clock speeds. This makes the MAC-1G ready to serve as a complete network controller that designers can simply connect to any 8-, 16-, 32-, or 64-bit processor working with any arbitrary clock frequency.

The MAC-1G can operate in 1-Gigabit mode (1000 Mbits/second) or in Fast Ethernet mode (10/100 Mbps) as directed by the host processor. Its network interface supports any PHY (physical layer) Ethernet device compliant with the 802.3 GMII/MII specification (Gigabit Media Independent Interface/Media Independent Interface). This enables it to work with all popular copper or fiber network connections, including 10Base-T, 100Base-TX, 100Base-FX, and 1000Base-T.

The core provides this functionality in a relatively compact package, as shown by the following reference design implementations (using the default core configuration optimized for speed, running at the standard Ethernet interface clock frequency of 125 MHz).

<u>Device/Technology</u>	<u>Area</u>	<u>Host Side Frequency</u>
Altera Stratix -7	5350 LCs	>100MHz
Xilinx Virtex E-8	2710 slices	>77MHz
Xilinx Virtex 2-6	2670 slices	>110MHz
UMC 0.18um ASIC	38600 gates	>125MHz

The MAC-1G provides full- or half-duplex operation, supports jumbo frames, offers statistical counters for Ethernet MIB (management information base), and includes features for low-power operation. Pre-synthesis options allow users to tailor the MAC-1G to their specific application, and custom versions of the core are available.

About the USB 2.0 Function Controller Core

The CUSB2 core implements a complete high-speed peripheral controller that interfaces to a USB port on one side and to a system's microprocessor on the other. Suitable for embedded microcontroller or communication system applications, it transfers data at 480 Mbps in compliance with the USB 2.0 specification, and is backward-compatible with the USB 1.1 full-speed (12 Mbps) rate. It is user-configurable for up to 15 IN and OUT endpoints, and includes power management and remote wake-up functions.

The USB port physical layer (PHY) interface supports transceivers using the popular UTMI (the USB 2.0 Transceiver Macrocell Interface) developed by Intel. Support for the Philips ISP1501 transceiver is an option.

The generic microprocessor interface is designed for straightforward integration with a variety of system architectures and bus types, and is configurable to work with 8-, 16-, or 32-bit processors. An optional configuration/enumeration FSM (finite state machine) is available to handle USB standard requests, relieving the host processor from servicing USB control transfers.

Reference designs show that a minimum configuration of the CUSB2 core for a 16-bit USB 2.0 transceiver data bus (UTMI clock = 30 Mhz) uses just 1012 slices in a Xilinx Virtex E-6, and 8700 gates in a TSMC 0.35um ASIC. (This typical minimum configuration includes endpoint 0 and two additional single buffered endpoints, IN and OUT, as might be used for a USB mass storage device.)

Both the CUSB2 and the MAC-1G cores were developed by CAST's primary technology partner Evatronix SA, based in Poland (www.evatronix.pl).

About CAST, Inc.

CAST provides general purpose IP (gplP), a broad range of popular and standards-based cores that includes processors, interfaces, and application-specific functions for multimedia and encryption. Designers use these cores so they can concentrate on the more unique, creative aspects of their system designs, or to quickly incorporate technology beyond their normal expertise.

Privately owned and operating since 1993 with a focus on making IP practical and affordable, the company has established a reputation for high-quality products, simple licensing, and responsive technical support. CAST is located near New York City, and works with an international network of IP developers and distributors.

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