

CAST Adds Ethernet MAC, 64-bit PCI, and CAN Controller to Line of General Purpose IP Cores

January 29, 2002, DesignCon, Santa Clara, California — Semiconductor intellectual property (IP) provider CAST, Inc. today announced the addition of four new cores to its line of general purpose IP for electronic design: the MAC Ethernet Media Access controller, the 64-bit PCI-T64 PCI Target and PCI-M64 Master/Target Interfaces, and the CAN Bus Controller.

"We already have one of the broadest available lines of IP cores, but customers have been asking for these specific functions," said Hal Barbour, president of CAST. "These new additions make our general purpose IP even more beneficial to SoC developers, who want to focus on designing their unique applications or product elements and rapidly assemble the rest of the system."

The new cores are available for license now, in hardware description language (HDL) form ready for synthesis to ASICs or for implementation with Altera or Xilinx FPGAs. Custom core modifications and other options are also available.

Expanding the General Purpose IP Product Line

The four new cores join a broad range of products that the company refers to as "general purpose IP," or GPIIP. This term distinguishes the product line from "star IP" — proprietary 32- or 64-bit processors and other high-end functions — and "commodity IP" — lower-end, often trailing-edge blocks and functions.

GPIIP also characterizes the breadth of CAST's core offerings, and its goal of serving as a single-source supplier for most popular or standards-based cores. Unlike other IP providers that specialize in one technological niche or another, CAST delivers a broad range of cores by augmenting its own development efforts with the expertise of international development partners. Each partner brings a special focus to the team, while CAST determines customer requirements, sets development and quality standards, and provides extensive customer support.

The new Ethernet MAC core, for example, was developed by primary partner Evatronix S.A. in Poland. The PCI cores were developed by CAST in the Czech Republic, while the CAN Controller comes from the Fraunhofer-Institute for Microelectronics in Germany.

Customers respond well to the GPIIP approach, counting on CAST's nine-year experience delivering high-quality models and IP and appreciating the ability to select many of the cores they need from one trusted source. Typical uses include achieving faster time to market by augmenting the more creative, proprietary portions of SoC designs, consolidating and enhancing existing board-based products with FPGAs or ASICs, and extending product lifetimes by replacing obsolete parts.

About the New Networking and Bus Controller Cores

The **MAC** core is a high-speed Ethernet local-area-network (LAN) controller based on the standard Intel/DEC 21143 chip. It implements Carrier Sense Multiple Access with Collision Detection (CSMA/CD) algorithms defined by the IEEE 802.3 standard for media access control over Ethernet. From the host side, the MAC uses a configurable interface for connecting external CPUs or standard bus controllers like a PCI. This interface can be configured to work with 8, 16 or 32 data bus lengths with big-endian or little-endian byte ordering.

The **PCI-T64 Target** and **PCI-M64 Master/Target** cores implement a 64-bit PCI interface, freeing the designer from this complex design task. Both support a 64-bit address/data bus, operate up to 66 MHz (PCI clock frequency), and are fully compliant with the PCI Local Bus Specification, Revision 2.2. Each implements 64 bytes of PCI Configuration Space registers, with the Configuration Space extendable up to 256 bytes if required. The target portions support up to six Base Address Registers with both I/O and Memory space decoding from 16 bytes up to 4 gigabytes.

The **CAN Bus Controller** core implements the CAN serial communications protocol. This widely accepted protocol was developed in response to the need for powerful field bus systems for distributed real-time networks in the face of increasingly complex microsystems. The CAN bus core is based on the basic CAN principle, and it meets all constraints of the CAN-specification 2.0B. Three 13-byte buffers are used for buffering of received or transmitted messages. In practice no overload frames will be generated.

About CAST, Inc.

CAST provides a broad line of general-purpose IP cores, including 8- and 16-bit processors, peripherals, buses, network interfaces, communications devices, multimedia operations, and encryption functions.

Self-owned and self-financed, the company's IP revenue grew 50% in 2001 due to its popular product line and lean operations model. Operating since 1993 with a focus on making IP practical and affordable for mainstream designers, the company has established a reputation for high-quality products, simple licensing, and responsive technical support. The company is located near New York City, and works with an international network of IP developers and distributors.

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