Munich, Germany—If the current growth trend continues, in a few years DATE—the yearly Design, Automation and Test in Europe forum—will be as big as the Design Automation Conference (DAC). At least, that's what the organizers of this year's electronic design forum were hoping when they made the announcement at DATE 2001 this month. While this year's event was much smaller than its American counterpart, a large number of new products were announced; some of which were also on view at last week's IP/SOC 2001 conference in Santa Clara, Calif.

**Design Entry**

Wilsonville, Ore.-based Mentor Graphics Corp. took the opportunity to introduce the HDL Designer Series, a new family of point tools for complex Verilog, VHDL or mixed language design, at DATE 2001. The tool suite combines technologies of the Mentor Graphics (nasdaq: MENT) Renoir HDL graphical entry tool with technology recently acquired from Escalade Corp. The HDL Designer Series features the company's patent-pending interface-based design (IBD) to solve the interconnect-creation problem. IBD is a text-based entry technology that displays design-interconnect structures in an easy-to-view and compact tabular format.

Closing the growing process-design gap between the physical process capabilities and the design complexity is Esterel Technologies SA of Guyancourt, France, which announced Esterel Studio 3.0. According to Esterel, system-level design is the only solution to this problem, but in order for it to be successful, system-level design must take into account application constraint at the behavioral level and be able to propagate these constraints along the design flow. The solution developed by Esterel is based on the company's language and combines formal methods with a full functional coverage of the designer's needs.

Frontier Design BVBA of Leuven, Belgium, announced enhancements to its A/RT Designer architectural synthesis tool, which provides a design flow from SystemC or C-language algorithms to optimized FPGA implementations. The new release supports C-language-based design for Virtex and Apex FPGAs and optimizes memory usage, as memory is a very expensive resource on FPGAs.

**Intellectual Property**

Woodcliff Lake, N.J.-based CAST Inc. and its development partner Evatronix SA of Bielsko-Biala, Poland, announced the release of two new synthesizable cores: the **C32025 DSP core**, compatible with the Texas Instruments Inc.'s **TMS320C25**, and the **CZ80CPU processor core**, compatible with the Zilog Z80.

Adaptive Silicon of Los Gatos, Calif., announced the first commercially available silicon intellectual property (IP) for embedded programmable logic. The core, called the **MSA 2500**, targets ASIC and ASSP system-on-a-chip (SOC) designs. Together with the core, the company also announced the Millennium PLC software environment that allows register transfer level (RTL) designs to be optimized for implementation into its programmable logic
Embedding a programmable logic core into an SOC gives designers the flexibility to modify the design after first silicon is produced, or to upgrade algorithms after the device has been shipped to a customer.

Improv Systems of Beverly, Mass., preannounced a new addition to its Acappella family of hardware/software solutions for voice-over-packet applications. The platform, based on the company’s configurable Jazz processor core, is optimized for voice-over-PacketCable, the standard created by CableLab for digital set-top boxes. Improv also preannounced new reference development boards for designing with the Jazz core.

**Verification**

TransEDA Plc. of Los Gatos announced that it has formed an SOC partnership with the Siemens AG Industrial Solutions and Services Group. Siemens has standardized on TransEDA's Verification Navigator integrated design environment, which will be used on all chip designs. Under the terms of the partnership, TransEDA will work closely with Siemens to help deploy Verification Navigator and to cooperate on the development of future verification technologies.

Certify SC (Single Chip) was announced by Synplicity, Sunnyvale, Calif. The tool, a new member of the company's Certify verification synthesis software family, is for ASIC and IP prototyping on a single FPGA. Compared to the pre-existing Certify tool, the Certify SC offers features such as the automatic conversion of ASIC's gated-clocks into the clock enable mechanism used in FPGAs. Synplicity (nasdaq: SYNP) also announced the integration of the Xilinx ChipScope debug technology into Certify SC, providing access to internal signals in the hardware debug phase.

Real Intent Inc., Santa Clara, Calif., announced that its Verix verification product supports VHDL and mixed Verilog/VHDL designs. The company also introduced a Verix version that runs on Red Hat Linux. Real Intent recently named ALT Technologies as its distributor for the United Kingdom and Ireland.

**EDA Hardware**

IKOS Systems Inc. of San Jose chose DATE to announce the fourth generation of its VStation-15M emulator, which provides users with up to 15 million usable ASIC gate capacity and performance up to 2MHz. The VStation-15M consists of nine array boards with Virtex V800 parts and features 100 percent visibility of all internal and external signals at any time. Henderson, Nev.-based Aldec Inc. announced the industry's first RTL simulation acceleration platform incorporating Incremental Prototyping methodology to verify multimillion-gate SOC designs. The technology was developed by Hardware Embedded Simulation (HES), a newly formed Aldec business unit. HES allows the designer to verify and optimize his or her design in manageable, smaller-sized blocks. Each block is simulated in software by a Design Verification Manager (DVM), before being pushed into an FPGA. Blocks remain connected by the DVM in software as they are in turn pushed into the FPGA. However, reverifications of the growing design are simulated in the FPGA hardware and are performed in milliseconds, not hours. This technology allows the designers to use the project's originally selected simulators, eliminating the need to apply a new learning curve.

**Physical Design**

Sequence Design Inc. preannounced Physical Studio, a physical optimization system for
SOC design closure below 180nm. Physical Studio addresses timing and signal-integrity problems caused by the fact that, below 180nm, wire-to-wire capacitance is larger than wire-to-chip capacitance. According to Santa Clara-based Sequence, Physical Studio produces 15 percent to 20 percent faster chips while solving signal-integrity problems.

The merger with Aristo Technology Inc. took center stage at the Monterey Design Systems Inc. booth. The deal will provide customers with an integrated physical design solution from design planning through full chip tapeout SOC designs of up to 100 million gates. Details of the merger have not been disclosed. The resulting company will retain the Monterey name.

Sunnyvale-based Monterey also announced Dolphin 1.5, the company's physical design solution, offering reduced memory usage and a significant performance increase. New features include IR-drop analysis for power and signal nets, electromagnetic-driven routing rules and automatic metal slotting to reduce stress in metal layers.

Test

SynTest Technologies Inc. of Sunnyvale announced a logic built-in self-test (BIST) tool called TurboBIST-Logic, for Verilog and VHDL designs. Based on the company's ATPG technology, the tool allows at-speed testing.

San Jose-based LogicVision (nasdaq: LTXX) announced a European center in Basingstoke, England, and launched new versions of its range of embedded test IP products. Capabilities now include coverage of defects that cause interference between ports in multiport RAMs.

Palo Alto-based Agilent Technologies Inc. (nyse: A) and Mountain View, Calif.-based Synopsys (nasdaq: SNPS) announced an agreement to reduce the overall cost of testing complex semiconductor devices. The two companies will explore the ability to make EDA test tools aware of intended automated test equipment (ATE) environments for SOC devices in order to synthesize the optimal design-for-test structure. Moreover, ATE hardware must have the ability to fully use every DFT resource available on the device.