

# CAST

## MAC-51\_AP

### Embedded Internet Application Platform

The MAC-51\_AP platform combines an 8-bit processor core, a 10/100 Mbps Ethernet MAC device controller core, a checksum hardware accelerator, and a third-party TCP/IP software stack to provide Internet connectivity for System on Chip (SoC) designs.

The application platform's pre-integrated CAST cores work together as a fast, compact, programmable Ethernet controller. The R8051XC2 Microcontroller Core executes the MCS@51 instruction set with just one clock per cycle, has numerous optional features and peripherals capabilities, and has been proven in hundreds of customer designs. The MAC-L Media Access Controller Core supports full- and half-duplex operation, has a Media Independent Interface (MII) for simple control, and includes a parameterized, multi-packet FIFO implemented using dual-port RAMs.

A custom Hardware Accelerator core also integrated in the application platform efficiently controls checksums for common TCP/IP protocols like TCP, IPv4, UDP and ICMP.

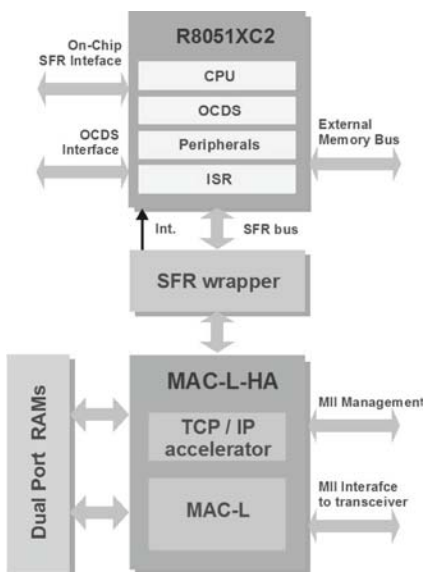
The MAC-51\_AP platform was proven with the CMX-Micronet™ TCP/IP software stack from CMX Systems, Inc. This features a MAC-L driver for optimum operation with the 8051 and Ethernet cores.

The application platform is designed for reuse in ASIC and FPGA implementations. The design is strictly synchronous with positive-edge clocking and a synchronous reset without internal tri-states; therefore, the scan insertion is straightforward.

### Applications

The pre-integrated, pre-verified platform is a good choice for easily bringing Internet connectivity to a variety of lower-end applications, including sensor modules, remote control & automation systems, point of sale terminals, weight systems for retail and bulk sales, and cash registers.

### Block Diagram



### Features

- Integrates CAST cores and adds software stack:
  - R8051XC2** 8-bit microcontroller core
  - MAC-L** 10/100 Mbps Ethernet Media Access Controller core
  - HA** checksum hardware accelerator
  - CMX-Micronet™** TCP/IP stack from CMX Systems, Inc.

### Platform Highlights

- Reduces need for Ethernet controller hardware knowledge
- Fast, compact implementation
- Hardware accelerator for checksum control processing increases throughput and frees 8051 cycles for system use
- Development board and evaluation system available

### R8051XC2 Microcontroller

- Fast, single clock per cycle CPU
- Flexible interfaces to program and data memories
- Rich set of optional and configurable peripherals
- On Chip Debug Support (optional)
- MAC registers mapped to SFR address space and dedicated interrupt for MAC events
- See R8051XC2 datasheet for details

### Ethernet MAC-L

- 10/100Mb/s data transfer rates; meets IEEE 802.3 CSMA/CD standard
- MII, RMII and SMII PHY compatibility
- Flexible address filtering, programmable FIFO threshold levels
- See MAC-L datasheet for details

### HA Hardware Accelerator

- Automatically discards bad frames, inserts checksums for IP/TCP/UDP/ICMP

### CMX-Micronet™ TCP/IP Software Stack

- Proven support of all popular protocols and functions
- Includes MAC-L driver optimized to forward checksum control to the hardware accelerator
- Visit the CMX website for full information:  
[www.cmx.com/micronet.htm](http://www.cmx.com/micronet.htm)

## Functional Description

The application platform is partitioned into modules as shown in the block diagram. The **CPU** performs arithmetic and logic functions, and includes various registers and interfaces. The **OCDS** block interfaces the core with optional, full-featured, native On-Chip Debug Support through an IEEE1149.1 (JTAG) port.

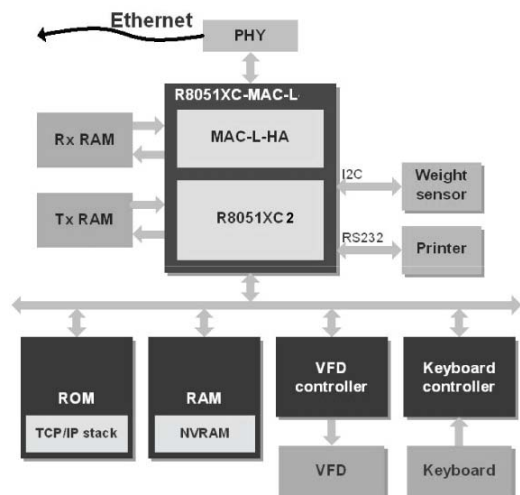
The **Peripherals** block is a fully configurable and easily adjustable set of components and peripherals (See the R8051XC2 datasheet for details.)

The **ISR** or Interrupt Service Routine block services up to 18 interrupt sources (besides the MAC-L interrupts) at four priority levels. The MAC-L interrupts are directly connected to R8051XC2 interrupt logic; they do not reduce the external interrupt inputs available to the user.

The **MAC-L-HA** block includes the MAC-L core and the Hardware Accelerator. The MAC-L implements Carrier Sense Multiple Access with Collision Detection (CSMA/CD) algorithms defined by the IEEE 802.3 standard for media access control over Ethernet. The HA automatically inserts and checks transmit and receive frame checksums for the TCP/IP/UDP/ICMP protocols. Specifics for each protocol can be set individually, and checksums for all protocols are computed on the fly. The **SFR Wrapper** block maps the MAC-L to the SFR.

## Example Application

This example application uses the platform's Ethernet connectivity to connect electronic scales to an in-store information system for automatic central database updating. It uses an intelligent weight sensor with I2C™ interface, a label printer with serial RS-232 interface, a Vacuum Fluorescent Display and its controller, and a Keyboard and Keyboard controller.



Example Application: Internet-Connected Electronic Scale System

## Options

- EDIF netlist for FPGA and low volume production
- Evaluation system based on EB5-Tiny Development Board
- Application-debugging Support Environment (EASE) that includes
  - Debug hardware for R8051XC2 controller
  - Software plug-in for Keil environment
  - Dedicated USB pod for data exchange device between debug hardware and personal computer
- R8051XC2 specific options:
  - Pre-configured R8051XC2-A and -B versions
  - Fully configurable version of R8051XC2 (R8051XC-F)

## Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

## Verification

All subcomponents were functionally verified with an HDL testbench using their individual test suites. The CPU and ALU have been verified against a proprietary hardware modeler and behavioral models. Hardware verification of the prototype was done with the aid of the CMX-MicroNet™ TCP/IP stack on a FPGA evaluation board.

## Deliverables

The core includes everything required for successful implementation:

- RTL source code (EDIF netlist available)
- Behavioral models for R8051XC CPU & Ethernet PHY
- An example chip implementation, which uses the application platform in a sample system
- Sophisticated HDL Testbench (Verilog versions use Verilog 2001)
- Simulation script, vectors, expected results, and comparison utility
- Synthesis script (ASICs) or place and route script (FPGAs)
- Comprehensive user documentation, including detailed specifications and a system integration guide.