JPEG2000-AP
JPEG2000 Encoding Application Platform

This JPEG2000 application platform integrates multiple IP cores with memory and software on a system prototyping board to enable off-the-shelf execution and evaluation of scalable, efficient compression of images at any resolution up to 64k x 64k pixels.

The JPEG2000 encoder, memory controller, and interface cores are implemented in an FPGA on a commercial board that has onboard RAM. The board connects to a Windows host PC via a PCI Express interface. Raw video is fed to the board through a virtual RAM drive, compressed, and passed back to the PC for storage and viewing.

The platform can compress greyscale images with a rate up to 100 MSamples/sec, and can be modified to support for even higher processing rates.

Custom software provides a graphical user interface (GUI) for easy setting of JPEG2000 compression parameters. It also manages video streaming, driver access, hardware control, and multitasking.

Applications
The application platform provides a turnkey solution for engineers needing to study JPEG2000 compression, develop and analyze a JPEG2000 proof of concept capability, or evaluate hardware JPEG2000 compression using their own imagery. The platform can also provide designers a head start on developing their own JPEG2000 systems.

Block Diagram

- Provides a complete, ready-to-use hardware/software package for JPEG2000 evaluation, proof of concept, or product development quick start.
- Up to 100 MSamples/sec and can be modified for higher processing rates.
- Enables easy evaluation of and experimentation with JPEG2000 video encoding using one’s own imagery.
- Provides a fast PCI Express interface to host computer (MS Windows 7, Vista, and XP).
- Integrates multiple CAST IP cores:
  - JPEG2000-E JPEG2000 Compression Encoder Core
  - DDR2-SDRAM-CTRL DDR/DDR2 SDRAM Memory Controller Core (if required)
  - CPXP-EP PCI Express Endpoint Controller Core
  - CCBB-AHB CAST AHB Compression Core Bus Bridge for JPEG2000-E Core
- Portable on commercial prototyping boards with Altera or Xilinx FPGAs. Of-the-shelf bit-streams available for:
  - Altera Stratix IV GX FPGA Development Kit
  - 5V330 TAI Logic Module from S2C, Inc. with Xilinx Virtex-5 FPGA for IP
- Includes essential software:
  - MS Windows Kernel-Mode Driver
  - GUI Control and Streaming Software
  - RAM Drive virtual disk utility to achieve input transfer rate sufficient for reading uncompressed imagery

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Functional Description

The JPEG2000-AP platform includes a number of IP cores and custom software modules as depicted in the block diagram. Key elements are described here.

PCI Express Host Interface

The application platform relies on a host computer first to transfer raw images to the system and then to receive, store, and display the compressed video output. PCI Express handles the necessary high transfer rate.

An included Application Interface module (PXP-AIF) interfaces the controller core with the internal bus (AMBA AHB). A Scatter-Gather extension (PXP-AIFSG) with a large memory buffer maximizes the efficiency of DMA data transfers between the AHB and PCI Express buses.

CCBB-AHB

The CCBB-AHB implements a simple interface between an AMBA™ AHB bus with the native Avalon ST I/O interfaces, and the configuration registers of the JPEG2000 core.

JPEG2000 Core

A single instantiation of the JPEG2000 encoder core configured to process tiles with size up to 1024x1024 is provided with the application platform. Other configurations of the JPEG2000 encoder core or instantiation of multiple cores for higher processing rates can be made available upon request.

Memory Controller

The memory controller is used to connect the JPEG2000 encoder core to an external memory. A DDR2 controller is included with the off-the-shelf configuration of the platform, but controllers for other memory type such as DDR3 can also be made available.

Software

The system includes a custom kernel-mode driver for MS Windows 7, Vista, and XP. Also, a custom GUI application handles driver access, hardware control, and multitasking.

Support

The system as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Verification

The system has been verified through simulation, code coverage measurements, and multiple live demonstrations.

Deliverables

The JPEG2000-AP is available with soft cores (synthesizable HDL) or firm cores (netlists) for FPGA technologies, and includes everything required for successful implementation:

- RTL source code or netlist
- Synthesis scripts
- Place & route scripts
- MS Windows Kernel-Mode driver
- GUI Control
- Comprehensive user documentation for the system and for each core, including detailed specifications, a system integration guide, and a demo guide.