

CAST

HDLC-51_AP

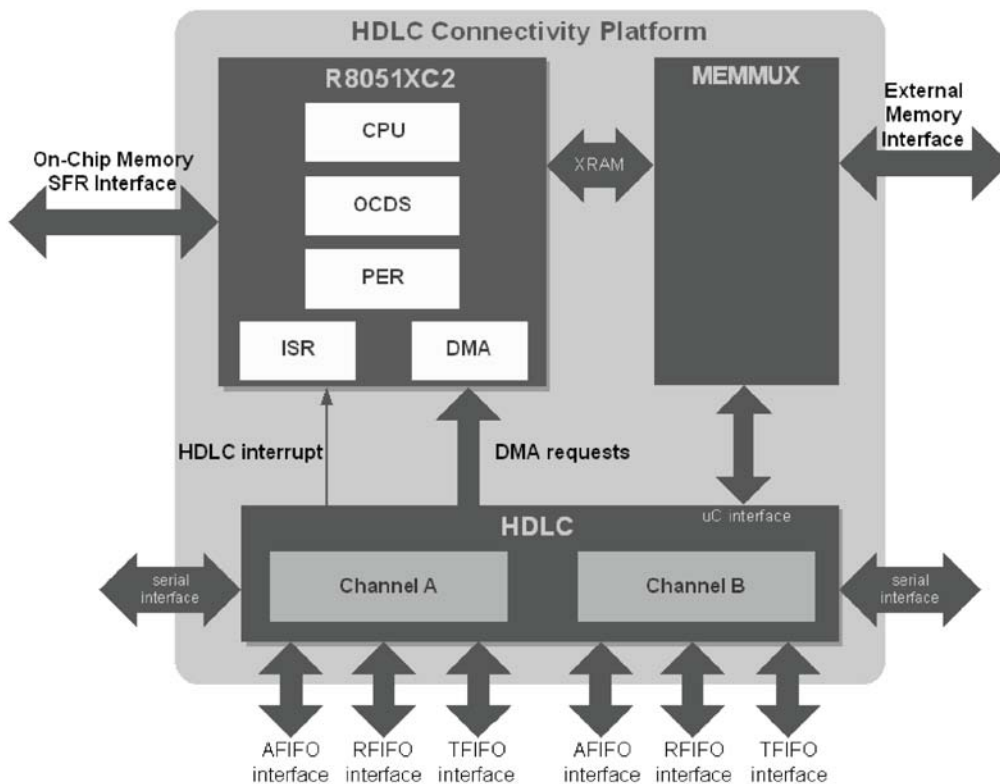
HDLC Connectivity Application Platform

The HDLC-51_AP is a ready-to-use platform that enables rapid development of both a complete HDLC protocol, and derivative-based solutions.

The HDLC Connectivity Application Platform integrates the R8051XC2 8-bit microcontroller with the HDLC Protocol Controller. The HDLC portion of the solution provides needed serialization and de-serialization, and it also supports automatic response generation for window size equal to 1. The R8051XC2 provides interrupts, interfaces for serial communication, timer system with compare-capture-reload resources, I/O ports, a power management unit, a multiplication-division unit, DMA controller, watchdog timer, and a real time clock. The extensive set of peripherals included can be easily modified to meet the requirements of a specific application.

The HDLC Connectivity Application Platform is a design developed for reuse in ASIC and FPGA implementations. The design is strictly synchronous with positive-edge clocking, no internal tri-states and with a synchronous reset; therefore scan insertion is straightforward.

Block Diagram



Features

Integrates CAST cores and adds software stack:

R8051XC2 8-bit microcontroller core

HDLC single- or dual-channel controller for the High-Level Data Link Control (HDLC) protocol and its derivatives

Platform Highlights

- Fast, compact implementation
- Hardware acceleration for LAPB/LAPD frees 8051 cycles for system use
- The R8051XC2 built-in DMA enables high throughput to the HDLC link
- Variety of configurable components make the HDLC-51_AP versatile and very customizable

R8051XC2 8-bit μ controller

- Fast single clock per cycle CPU
- Flexible interfaces to program and data memories
- Extensive set of optional and configurable peripherals
- On-chip Debug Support unit (optional)
- External memory interface
- Multiplication-Division Unit
- Special Function Registers interface
- Interrupt Controller
- Power Management Unit
- DMA Controller
- 16 Bit Timers/Counters
- SPI Master/Slave interface
- One or two I2C™ Master/Slave interfaces

HDLC Protocol Controller

- Two independent HDLC channels
- LAPB/LAPD controlling machine
- Serial Peripheral Interfaces
- Receive Length Check
- Three modes of receive operation
- Receive and transmit blocks
- Separate FIFOs

Applications

The pre-integrated, pre-verified platform is a good choice for easily bringing Internet connectivity to a variety of general purpose telecommunication applications, including X.25 link control, and ISDN applications.

Performance

The HDLC Connectivity Platform targets designers looking for a powerful 8-bit microcontroller integrated with an HDLC protocol controller.

The architecture eliminates redundant bus states and implements parallel processing of fetch and execution phases. Since a CPU cycle is aligned with memory fetch when possible, most of the 1-byte instructions are performed in a single cycle. The R8051XC2 uses 1 clock per cycle. This, together with other extensions (mutli-DPTR, MDU), leads to performance improvement at the rate of 12 (in terms of DMIPS), with respect to the Intel device working with the same clock frequency.

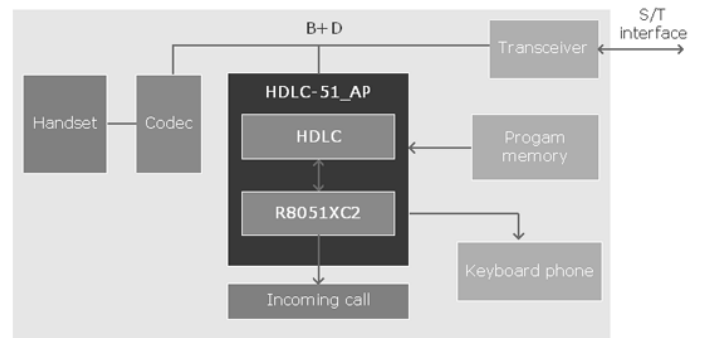
Verification Methods

The HDLC Connectivity Platform has been verified through extensive functional simulation and prototyped in an FPGA-based application.

The functional verification of subcomponents was performed in an HDL testbench. All subcomponents of R8051XC2 were verified together in the same testbench environment, even though the most important ones have individual test suites. The R8051XC2-CPU with an arithmetic-logic unit was verified against behavioral models, as well as a hardware model developed with a proprietary hardware modeler.

The peripherals, including the HDLC Protocol Controller IP core, have also been verified in their own testbenches, based either on hardware or behavioral models.

Example Application



This example application uses the platform's the R8051XC2 as a system MCU and the HDLC Protocol Controller for LAPD support to implement an ISDN phone. By using a time slot clock mode, the HDLC Protocol controller can be connected to multiplexed bus containing B and D channels.

Support

The platform as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Deliverables

The core includes everything required for successful implementation. The ASIC version includes:

- HDL RTL source code
- An example chip design
 - Integrates the R8051XC2 with HDLC
 - Illustrates how to build and connect interrupt signals, memories and port modules
- Sophisticated self-checking Testbench (Verilog versions use Verilog 2001) that instantiates example design, external RAM, clock generator, program memory model with random code generation mode, and monitors that compare simulation results with expected results
- A collection of 8051 assembler programs that are executed directly the Test Bench.
- Simulation script, vectors, expected results, and comparison utility
- Synthesis script
- Comprehensive user documentation, including detailed specifications and a system integration guide