

CAST

H264-AP

H.264 Encoding Application Platform

This H.264 application platform integrates multiple IP cores with memory and software on a system prototyping board to enable off-the-shelf execution and evaluation of high-definition video compression.

The H.264 encoder, memory controller, and interface cores are implemented in an FPGA on a commercial board that has onboard RAM. The board connects to a Windows host PC via a PCI Express interface. Raw video is fed to the board through a virtual RAM drive, compressed, and passed back to the PC for storage and viewing.

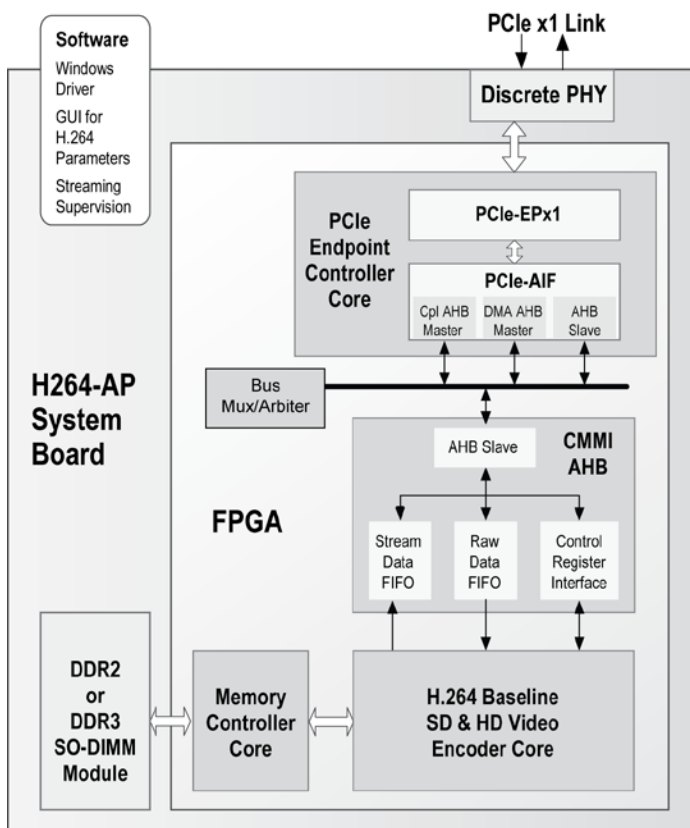
The system can process up to 1080p video at 30 frames per second.

Custom software provides a graphical user interface (GUI) for easy setting of H.264 compression parameters. It also manages video streaming, driver access, hardware control, and multitasking.

Applications

The application platform provides a turnkey solution for engineers needing to study and investigate H.264 video compression, develop and analyze an H.264 proof of concept capability, or evaluate hardware H.264 compression using their own video material. The platform can also provide designers a head start on developing their own H.264 systems.

Block Diagram



Features

- Provides a complete, ready-to-use hardware/software package for H.264 evaluation, proof of concept, or product development quick start.
- Processes up to 1080p video (1920 x 1080 pixel frames) at up to 30 fps.
- Enables easy evaluation of and experimentation with H.264 video encoding using one's own images and video.
- Provides a fast PCI Express interface to host computer (MS Windows 7, Vista, and XP).
- Integrates multiple CAST IP cores:
 - **H264-E** H.264/AVS SD & HD Video Encoder Core
 - **DDR2-SDRAM-CTRL** DDR/DDR2 SDRAM Memory Controller Core (if required)
 - **CPXP-EP** PCI Express Endpoint Controller Core
 - **CMMI-H264-E** CAST Multimedia Interface for H.264 Core
- Built on commercial prototyping boards with Altera or Xilinx FPGAs:
 - Altera Stratix IV GX FPGA Development Kit
 - 5V330 TAI Logic Module from S2C, Inc. with Xilinx Virtex-5 FPGA for IP
- Includes essential software:
 - MS Windows Kernel-Mode Driver
 - GUI Control and Streaming Software
 - RAM Drive virtual disk utility to achieve input transfer rate sufficient for reading uncompressed HD video

Functional Description

The H264-AP application platform includes a number of IP cores and custom software modules as depicted in the block diagram. Key elements are described here.

PCI Express Host Interface

The application platform relies on a host computer first to transfer a raw video stream to the system and then to receive, store, and display the compressed video output. PCI Express handles the necessary high transfer rate. An included Application Interface module (PCIe-AIF) interfaces the controller core with the internal bus (AMBA AHB). A Scatter-Gather extension (PXP-AIFSG) with a large memory buffer maximizes the efficiency of DMA data transfers between the AHB and PCI Express buses.

CMMI-AHB

The CMMI-AHB core bridges the AHB bus with the native Avalon ST I/O interfaces, and the configuration registers of the H264-E core,

Memory Controller

The memory controller is used to connect the H.264 encoder core to an external memory. A DDR2 controller is included with the off-the-shelf configuration of the platform, but controllers for other memory type such as DDR3 can also be made available.

Driver, Control, and GUI Software

The system includes a custom kernel-mode driver for MS Windows 7, Vista, and XP.

A custom GUI control and streaming application handles output streaming, driver access, hardware control, and multitasking (see figure). Three parallel threads ensure smooth video streaming: one manages the raw video data write to the hardware encoder, one reads the encoded stream from the hardware, and the third handles the correct video streaming.

Support

The system as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

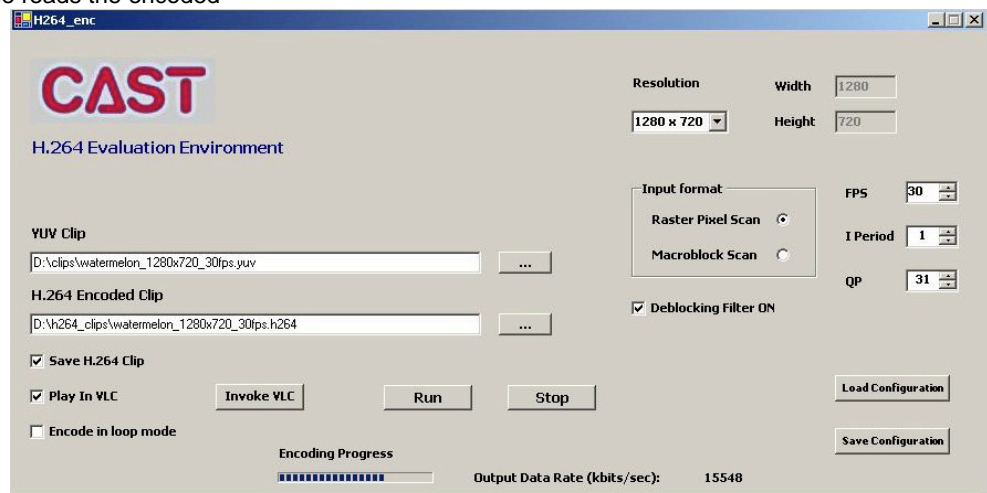
Verification

The system has been verified through simulation, code coverage measurements, and multiple live demonstrations.

Deliverables

The H264-AP is available with soft cores (synthesizable HDL) or firm cores (netlists) for FPGA technologies, and includes everything required for successful implementation.:

- HDL (VHDL or Verilog) RTL source code or netlist
- Synthesis scripts
- Place & route scripts
- MS Windows Kernel-Mode driver
- GUI Control and Streaming software
- Hardware as appropriate (board, PCIe PHY, PCIe cable with ExpressCard Adapter, System ACE)
- Comprehensive user documentation for the system and for each core, including detailed specifications, a system integration guide, and a demo guide.



CAST
info@cast-inc.com
www.cast-inc.com

CAST, Inc. 11 Stonewall Court
Woodcliff Lake, NJ 07677 USA
tel 201-391-8300 fax 201-391-8694
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Some cores in this application platform are sourced from Technology Partner [Alma Technologies](#).